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(54) SEMICONDUCTOR STORAGE DEVICE AND METHOD FOR MANUFACTURING THE SAME

(57) Abstract: PROBLEM TO BE SOLVED: To provide a nonvolatile semiconductor storage device for storing information for plural bits, using a simple cell structure.SOLUTION: In this new structure of a nonvolatile semiconductor storage device for storing information for plural bits, the edge part of a gate electrode is provided with a charge-storing layer 4 for storing electrons. Thus, information on plural bits can be stored by storing the electrons in the charge storage layer 4.

[Claim(s)]
[Claim 1] A nonvolatile semiconductor memory characterized by having
a 1st gate electrode arranged via a gate insulator layer on the principal plane of a semiconductor substrate,
the aforementioned charge accumulation layer arranged on the side face of said 1st gate electrode,
a 2nd gate electrode on the side face of said 1st gate electrode with the charge accumulation layer inbetween, and
an electric conduction layer which connects electrically said 1st and 2nd gate electrodes.

[Claim 2] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms the 1st gate electrode over a gate insulator layer on the principal plane of a semiconductor substrate,
the process which forms a charge accumulation layer and the 2nd gate electrode one by one on the side face of said 1st gate electrode, and
the gate electrode of the above 1st and the gate electrode of the above 2nd.
the process which forms the electric conduction layer which connects electrically

[Claim 3] The nonvolatile semiconductor memory characterized by having
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of a semiconductor substrate,
the charge accumulation layer arranged at the edge of the 2nd aforementioned insulator layer, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 4] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process of forming the 1st, the 2nd, and 3rd insulator layers one by one in this order on the principal plane top of a semiconductor substrate and which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers,
the process which forms a gate electrode by carrying out patterning of this gate electrode component and a gate insulator layer after depositing a gate electrode component on the upper part of this gate insulator layer,
the process which removes the edge of the 2nd aforementioned insulator layer alternatively and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 5] The semiconductor memory characterized by providing
the nonvolatile semiconductor memory which has
the 1st lower insulator layer arranged on the principal plane of a semiconductor substrate,
the 1st middle insulator layer arranged at the upper part of the center of the 1st lower insulator layer,
the 1st charge accumulation layer arranged at the upper part of the edge of the above 1st lower insulator layer,
the 1st upper insulator layer arranged at the upper part of the above 1st middle insulator layer and the 1st charge accumulation layer, and
the 1st gate electrode arranged at the upper part of the 1st up insulator layer
and
the volatile semiconductor memory which has
the 2nd lower insulator layer which has been arranged on the principal plane of the aforementioned semiconductor substrate and which consists of the same material as the interval insulator layer of the above 1st,
the ultra-thin insulator layer arranged on the principal plane top of the aforementioned semiconductor substrate and to the ends of the 2nd lower insulator layer,
the 2nd charge accumulation layer which has been arranged at the upper part of this ultra-thin

insulator layer and which consists of the same material as the above 1st charge accumulation layer,
the 2nd upper insulator layer which has been arranged at the upper part of the above 2nd lower insulator layer and the 2nd charge accumulation layer and which consists of the same material as the above 1st upper insulator layer, and
the 2nd gate electrode arranged at the upper part of the 2nd upper insulator layer.

[Claim 6] the semiconductor memory characterized by providing
the nonvolatile semiconductor memory which has
the 1st lower insulator layer arranged on the principal plane of a semiconductor substrate
the 1st middle insulator layer arranged at the upper part of the center of the 1st lower insulator layer,
the 1st charge accumulation layer arranged at the upper part of the edges of the above 1st lower insulator layer,
the 1st upper insulator layer arranged at the upper part of the above 1st interval insulator layer and the 1st charge accumulation layer, and
the 1st gate electrode arranged at the upper part of the 1st upper insulator layer,
and
the volatile semiconductor memory which has
the ultra-thin insulator layer arranged on the principal plane of the aforementioned semiconductor substrate,
the 2nd charge accumulation layer which has been arranged on this ultra-thin insulator layer and which consists of the same material as the above 1st charge accumulation layer,
the 2nd upper insulator layer arranged on the 2nd charge accumulation layer, and
the 2nd gate electrode arranged on the 2nd upper insulator layer.

[Claim 7] The volatile semiconductor memory characterized by having
the lower insulator layer which has been arranged on the principal plane of a semiconductor substrate,
the ultra-thin insulator layer arranged on top of the principal plane of the aforementioned semiconductor substrate and at the ends of this lower insulator layer,
the charge accumulation layer arranged at the upper part of this ultra-thin insulator layer,
the upper insulator layer arranged on top of the aforementioned lower insulator layer and a charge accumulation layer, and
the gate electrode arranged at the upper part of this up insulator layer .

[Claim 8] The volatile semiconductor memory characterized by having
the ultra-thin insulator layer arranged on the principal plane of a semiconductor substrate,
the charge accumulation layer arranged on this ultra-thin insulator layer,
the insulator layer arranged on this charge accumulation layer, and
the gate electrode arranged on this insulator layer.

[Claim 9] The semiconductor memory characterized by including at least
the process which forms the 1st insulator layer on part of the principal plane of a semiconductor substrate,
the process which forms the 2nd and 3rd insulator layers one by one in the part other than on the principal plane of the aforementioned semiconductor substrate and the upper part of this 1st insulator layer,
the process which deposits a gate electrode component on the upper part of this 3rd insulator layer,
the process which forms the 1st gate electrode by carrying out patterning of this gate electrode component, the 3rd aforementioned insulator layer, the 2nd aforementioned insulator layer and the 1st insulator layer,
the process which forms the 2nd gate electrode by carrying out patterning of the aforementioned gate electrode component, the aforementioned 3rd insulator layer and the 2nd insulator layer,
the manufacture technique process which removes alternatively the edge of the 2nd insulator

layer of both the 1st and 2nd gate electrodes, and thereby forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 10] The manufacture technique of the semiconductor memory characterized by including at least
the process which forms the 1st, the 2nd, and 3rd insulator layers one by one on the principal plane of a semiconductor substrate,
the process which forms the 1st gate electrode by carrying out patterning this gate electrode component, the 3rd aforementioned insulator layer, the 2nd aforementioned insulator layer and the 1st insulator layer after depositing the 1st gate electrode component on the upper part of this 3rd insulator layer,
the process which forms the 2nd gate electrode formation field by removing the aforementioned gate electrode component, the 3rd aforementioned insulator layer, the 2nd aforementioned insulator layer and the 1st insulator layer of part of principal plane of the aforementioned semiconductor substrate, the process being simultaneously process performed with the 1st gate electrode formation process,
the process which removes alternatively the edge of the 2nd insulator layer of the above 1st gate electrode, and forms space,
the process which forms an ultra-thin insulator layer on the principal plane of the aforementioned semiconductor substrate,
the process which forms a charge accumulation layer in the space of the above 1st gate electrode by carrying out anisotropic etching of this charge accumulation layer component after depositing the material which constitutes a charge accumulation layer
the process which forms the 2nd gate electrode by carrying out patterning of the 2nd gate electrode component, the aforementioned 4th insulator layer, aforementioned charge accumulation layer component and ultra-thin insulator layer, after depositing the 4th insulator layer and the 2nd gate electrode component on the principal plane of the aforementioned semiconductor substrate.

[Claim 11] The nonvolatile semiconductor memory characterized by having
the heights arranged on the principal plane of a semiconductor substrate,
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing these heights,
the charge accumulation layer arranged at the edge of the 2nd aforementioned insulator layer, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 12] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a heights on the principal plane of a semiconductor substrate,
the process which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers by forming the 1st, the 2nd, and 3rd insulator layers one by one on the aforementioned semiconductor substrate containing these heights,
the process which forms a gate electrode by carrying out patterning of this gate electrode component and a gate insulator layer after depositing a gate electrode component on the upper part of this gate insulator layer,
the process which removes the edge of the 2nd aforementioned insulator layer alternatively, and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 13] The nonvolatile semiconductor memory characterized by having
the heights arranged on the principal plane of a semiconductor substrate, and
the gate insulator layer which consists of the 1st and 2nd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing this heights,
the charge accumulation layer arranged between the 1st and 2nd insulator layers, and
the gate electrode arranged on the aforementioned gate insulator layer

[Claim 14] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a heights on the principal plane of a semiconductor substrate,
the process that forms the 1st insulator layer, a charge accumulation layer component and the 3rd insulator layer one by one, on the aforementioned semiconductor substrate containing this heights, and
the process which forms a gate electrode by carrying out patterning of this 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer.

[Claim 15] The nonvolatile semiconductor memory characterized by having
the concavity arranged on the principal plane of a semiconductor substrate,
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing this concavity,
the charge accumulation layer arranged at the edge of the aforementioned 2nd insulator layer, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 16] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate,
the process which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers, by forming the 1st, the 2nd, and 3rd insulator layers one by one on the aforementioned semiconductor substrate containing this concavity,
the process which forms a gate electrode by carrying out patterning of this gate electrode component and a gate insulator layer after depositing a gate electrode component on the upper part of this gate insulator layer,
the process which removes the edge of the 2nd aforementioned insulator layer alternatively, and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 17] The nonvolatile semiconductor memory characterized by having
the concavity arranged on the principal plane of a semiconductor substrate,
the gate insulator layer which consists of the 1st and 2nd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing this concavity,
the charge accumulation layer arranged between the 1st and 2nd insulator layers, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 18] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate,
the process that forms the 1st insulator layer, a charge accumulation layer component and the 3rd insulator layer, one by one, on the aforementioned semiconductor substrate containing this heights,
the process which forms a gate electrode by carrying out patterning of this 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer.

[Claim 19] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate,
the process which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers by forming the 1st, the 2nd, and 3rd insulator layers one by one on the aforementioned semiconductor substrate containing this concavity,
the process which forms the gate electrode embedded at the aforementioned concavity by removing this gate electrode component by the chemical mechanical polishing technique after depositing a gate electrode component on the upper part of this gate insulator layer,

the process which removes the edge of the aforementioned 2nd insulator layer alternatively, and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 20] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate, and
the process which forms the 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer one by one on the principal plane of the aforementioned semiconductor substrate containing this concavity,
the process which forms the gate electrode embedded at the aforementioned concavity by removing this gate electrode component by the chemical mechanical polishing technique after depositing a gate electrode component on the upper part of this 3rd insulator layer.

[Claim 21] The nonvolatile semiconductor memory characterized by having
the gate electrode arranged through a gate insulator layer on the principal plane of a semiconductor substrate,
the concavity arranged at the edge of this gate electrode, and
the charge accumulation layer arranged through an insulator layer in the upper part of both a channel field and a source drain field at this concavity.

[Detailed Description of the Invention]

[0001] [The technical field to which invention belongs]
This invention relates to an electrically programmable and erasable nonvolatile semiconductor memory and its manufacture technique, a high speed programmable and readable volatile semiconductor memory and its manufacture technique, and a semiconductor memory having a nonvolatile semiconductor memory and a volatile semiconductor memory on the same chip, and its manufacture technique.

[0002] [Description of the Prior Art]
In non-volatile memories, such as conventional EEPROMs (Electrically Erasable and Programmable Read Only Memory), a 1 bit information is memorized in one cell by realizing two different thresholds in one cell.
On the other hand, for the formation of memory high-density, four or more thresholds are given to one cell, and the technique of memorizing the above information in one cell by 2 bits is proposed (M. Bauer et al., ISSCC95, and p.132).
However, in order to realize this technique, an exact control of the threshold voltages, the exact detection for small changes of threshold voltage, and further, a charge hold reliability more than the former are required.
Therefore, with this technique, a performance equivalent to the former can actually not necessarily be obtained.
Moreover, this technique also has the problem, that the manufacture yield is low.
For this reason, the cellular structure which memorizes a plurality of bit information by accumulating a charge in a plurality of physically different positions is newly proposed (B. Eitan et al, IEDM96, p169, and Fig. 6).
Moreover, as a similar cellular structure to this, a structure providing a charge accumulation layer on the side wall of the gate electrode has been proposed by this invention person before (U.S. patent number of No. 4881108).
However, the manufacturing process of these cellular structures is very complicated, and has the problem that the controllability of a channel field is not enough, either.

[0003] On the other hand, from the demand for system-on-chips of these days, the necessity of realizing an electrically writing-in erasable non-volatile memory and a high speed writing-in read-out erasable volatile memory on the same chip is increasing.
Especially, the demand for VLSI, which combine a high speed operation dynamic RAM and a non-volatile memory with a floating-gate structure such as EEPROM and flash memory, is increasing rapidly.
However, the memory cell of a dynamic RAM in recent years has very complicated three-dimensional structure called trench structure and stack structure.
For this reason, if it is going to combine floating-gate type non-volatile memory and a dynamic RAM, from the difference in the memory cell structure, a manufacture process will be complicated and the number of mask processes will also increase.
Therefore, the manufacturing cost of the combined chip will become very big.

[0004] If the memory cell of a dynamic RAM is realized using the memory cell structure of non-volatilized floating-gate type memory, it is possible for a manufacture process to be simplified by communalization of the cellular structure and to reduce a manufacturing cost by it.
However, in the communalized memory cell, it is difficult to realize the high-speed writing which is the characteristic feature of a dynamic RAM.

[0005] [Problem(s) to be Solved by the Invention]
This invention is accomplished in view of the above-mentioned situation, and aims at offering the structure of the nonvolatile semiconductor memory which can memorize the two or more bit information with an easy cellular structure.

[0006] Other purposes of this invention are offering the manufacture technique of the nonvolatile

semiconductor memory which manufactures the nonvolatile semiconductor memory which memorizes a two or more bit information in an easy manufacture process.

[0007] The further other purpose of this invention is offering the structure of a semiconductor memory with an easy cellular structure having an electrically programmable erasable non-volatile memory and a high-speed read-out write-in volatile memory combined.

[0008] The further other purpose of this invention is offering the manufacture technique of a semiconductor memory with an easy manufacture process having an electrically programmable erasable non-volatile memory and a high-speed read-out write-in volatile memory combined.

[0009] [Means for Solving the Problem]
In order to attain the above-mentioned purpose, the 1st characteristic feature of this invention is a nonvolatile semiconductor memory comprising at least
a 1st gate electrode arranged on the principal plane of a semiconductor substrate with a gate insulator layer in-between the two,
a charge accumulation layer on the side face of the 1st gate electrode,
a 2nd gate electrode on the 1st gate electrode with the charge accumulation layer in-between the two,
an electric conduction layer electrically connecting the 1st gate electrode and the 2nd gate electrode.

[0010] The 2nd characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of a semiconductor substrate,
the charge accumulation layer arranged at the edge of the 2nd insulator layer, and
the gate electrode arranged on the gate insulator layer.

[0011] The 3rd characteristic feature of this invention is a semiconductor memory combining a nonvolatile semiconductor memory and a volatile semiconductor memory,
the nonvolatile semiconductor memory comprising at least
a 1st lower insulator layer arranged on the principal plane of the semiconductor substrate, and
a 1st interval insulator layer arranged at the upper part of the center of the 1st lower insulator layer,
the 1st up insulator layer arranged at the upper part of the 1st charge accumulation layer arranged at the upper part of the edge of the 1st lower insulator layer, and
the 1st interval insulator layer and the 1st charge accumulation layer,
the 1st gate electrode arranged at the upper part of the 1st up insulator layer,
the volatile semiconductor memory comprising at least
a 2nd lower insulator layer which has been arranged on the principal plane of the semiconductor substrate and which consists of the same material as the 1st interval insulator layer,
on the principal plane of a semiconductor substrate, and
the ultra-thin insulator layer arranged to the ends of the 2nd lower insulator layer,
the 2nd charge accumulation layer which has been arranged at the upper part of an ultra-thin insulator layer and which consists of the same material as the 1st charge accumulation layer,
the 2nd gate electrode arranged at the upper part of the 2nd up insulator layer which has been arranged at the upper part of the 2nd lower insulator layer and the 2nd charge accumulation layer, and which consists of the same material as the 1st up insulator layer, and the 2nd up insulator layer.

[0012] The 4th characteristic feature of this invention is a semiconductor memory which combines a nonvolatile semiconductor memory and an volatile semiconductor memory, the nonvolatile semiconductor memory comprising at least the 1st lower insulator layer arranged on the principal plane of a semiconductor substrate, and the 1st interval insulator layer arranged at the upper part of the center of the 1st lower insulator layer, the 1st up insulator layer arranged at

the upper part of the 1st charge accumulation layer arranged at the upper part of the edge of the 1st lower insulator layer, and the 1st interval insulator layer and the 1st charge accumulation layer, the 1st gate electrode arranged at the upper part of the 1st up insulator layer, an volatile semiconductor memory comprising at least the 2nd charge accumulation layer which has been arranged on the ultra-thin insulator layer arranged on the principal plane of a semiconductor substrate, and an ultra-thin insulator layer and which consists of the same material as the 1st charge accumulation layer, the 2nd gate electrode arranged on the 2nd up insulator layer arranged on the 2nd charge accumulation layer and the 2nd up insulator layer.

[0013] The 5th characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of the semiconductor substrate containing the heights or concavity arranged on the principal plane of a semiconductor substrate, and a heights or a concavity, the charge accumulation layer arranged at the edge of the 2nd insulator layer, and a gate electrode arranged on the gate insulator layer.

[0014] The 6th characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least the charge accumulation layer arranged between the gate insulator layer which consists of the 1st and 2nd insulator layers arranged on the principal plane of the semiconductor substrate containing the heights or concavity arranged on the principal plane of a semiconductor substrate, and a heights or a concavity, and the 1st and 2nd insulator layers, and the gate electrode arranged on a gate insulator layer.

[0015] The 7th characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least the gate electrode arranged on the principal plane of a semiconductor substrate with a gate insulator layer inbetween, the concavity arranged at the edge of a gate electrode, the charge accumulation layer arranged at the concavity with an insulator layer inbetween, and a charge accumulation layer arranged at the upper part of both a channel field and a source drain field.

[0016] [Embodiments of the Invention]
With reference to a drawing, the embodiment forms of this invention are explained below.
In the publication of the following drawings, the same or similar sign is given to the same or similar fraction.
However, a drawing is typical and the proportion of the relation between thickness and a flat-surface dimension and the thickness of each class etc. should regard differing from an actual thing.
Therefore, in consideration of the following explanations, you should judge concrete thickness and a concrete dimension.
Moreover, of course, between drawings the fraction from which the relation and proportion of a mutual dimension, also contain differences.

[0017] (1st Embodiment Form) Fig. 1 is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.
This memory cell consists of an n type MOS transistor.
With the memory cell structure of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention, the 1st gate electrode 3 is formed in the front face of the p type semiconductor substrate 1 through the gate insulator layer 2, and the charge accumulation layer 4 (4a, 4b) is formed on both sides of the 1st gate electrode 3.
This charge accumulation layer 4 has the laminated structure, the 1st layer is oxide film 5, the 2nd layer consist of a nitride 6, and the 3rd layer consists of the 2nd oxide film 7.
Furthermore, the 2nd gate electrode 8 is formed in the upper part of the charge accumulation layer 4.
The side wall spacer 9 is formed in the side face of the charge accumulation layer 4,
and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n-

type diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each front face of the 1st gate electrode 3, the charge accumulation layer 4, the 2nd gate electrode 8, and n+ type diffusion layer 11.
The 1st gate electrode 3 and the 2nd gate electrode 8 are electrically connected through this electric conduction layer 12.

[0018] The memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention has LDD (Lightly Doped Drain) structure which constituted the source field and the drain field, from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration.
And then, the charge accumulation layer 4 is formed in the both sides of 1st gate electrode 3, and the threshold change of potential, which is produced according to the existence of the electron held at the nitride layer 6 of these two charge accumulation layers 4, this threshold change of potential is made to correspond to a storage information "00", "01", "10", and "11".
Furthermore, the 2nd gate electrode 8 is formed in the upper part of the charge accumulation layer 4, by electrically connecting this 2nd gate electrode 8 to the 1st gate electrode 3, the controllability of a channel field is raised and detection for threshold voltage change is made easy.

[0019] Next, an operation of the non-volatile memory concerning the 1st embodiment form of this invention is explained using Fig. 2 to Fig. 4 .
Fig. 2 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 3 is a cross section of the non-volatile memory explaining a read-out operation.
Fig. 4 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 2 , at the time of the writing of a memory cell, the high voltage (-10V) is impressed to gate G, and simultaneously, the high voltage (-8V) is applied to drain D in the proximity of charge accumulation layer 4b which accumulates an electron, and the non-proximity source S is grounded.
Thus, if a voltage is impressed, a channel thermoelectron (Channel Hot Electron) will occur and this thermoelectron will be captured by the nitride 6 of charge accumulation layer 4b.
When the charge accumulation layer 4b captures an electron, the threshold voltage of a cell transistor changes.
Read-out of a memory cell is performed by detecting a part for a threshold change of potential.
Specifically, as shown in Fig. 3 , voltage 5V are added to gate G, voltage 3V are simultaneously impressed to drain D, and the difference of the amount of currents is detected with a sense amplifier.
Moreover, as shown in Fig. 4 , a deletion of a memory cell is performed by impressing a negative voltage (at least - 6V) to gate G, a right voltage (9V) to drain D in the proximity of charge accumulation layer 4b to be erased, and by emitting trapped electron of charge accumulation layer 4b.
In addition, as everyone knows, source S and drain D of an MOS transistor are made symmetrically, and, generally source S and drain D can be changed.
Therefore, also in the above-mentioned explanation, it is possible to replace source S and drain D.

[0020] Next, the manufacture technique of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention is explained using Fig. 5 through Fig. 9 .
As first shown in Fig. 5 , the 25nm gate insulator layer 2 is formed by thermal oxidation on the p type semiconductor substrate 1.
Then, after depositing the 300nm polycrystal silicon layer which is doped by n type or p type impurity by the LPCVD (Low Pressure Chemical Vapor Deposition) method all over p type semiconductor substrate 1, patterning is carried out with well-known exposure technique and well-known etching technique, and the 1st gate electrode 3 is formed.

[0021] Next, as shown in Fig. 6 , after removing the gate insulator layer 2 of the front face of the p type semiconductor substrate 1 of the field which forms a source field and a drain field, the p type semiconductor substrate 1 is oxidized thermally in a 900 degrees C - 1200 degrees C oxidizing atmosphere, and the 1st 10nm oxide film 5 is formed.
And the 10nm - 100nm nitride 6 is deposited by the LPCVD method on the 1st oxide film 5, and after that, the 2nd about 5nm oxide film 7 is formed in nitride 6 front face by 900-degree C hydrogen-burning oxidization or CVD.

[0022] Next, as shown in Fig. 7 , after depositing about 25-250nm polycrystal silicon on the 2nd oxide film 7 by the LPCVD method for example, anisotropic etching by the RIE (Reactive Ion Etching) method is performed, and by removing of this polycrystal silicon layer, the 1st oxide film 5, the nitride 6, and the 2nd oxide film 7 only their film thickness part, the charge accumulation layer 4 which has the 2nd gate electrode 8 in the upper part is formed at the 1st gate electrode side face.

[0023] Next, as shown in Fig. 8 , n- type diffusion layer 10 of low impurity concentration is formed.
It is formed by ion-implantation technique, that is by pouring in n type impurity using the 1st gate electrode 3 and the charge accumulation layer 4 as the mask, and by activating the impurity which was poured in by subsequent heat treatment.

[0024] Next, as shown in Fig. 9 , after forming the side wall spacer 9 in the side wall of the charge accumulation layer 4, n+ type diffusion layer 11 of high impurity concentration is formed.
It is formed by ion-implantation technique, that is by pouring in n type impurity using the 1st gate electrode 3, the charge accumulation layer 4 and the side wall spacer 9 as the mask, and by activating the impurity which was poured in by subsequent heat treatment.

[0025] Next, high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, and then, by heat-treating the p type semiconductor substrate 1 in an inert atmosphere in each front face of the 1st gate electrode 3, the charge accumulation layer 4, the 2nd gate electrode 8, and n+ type diffusion layer 11, the electric conduction layer 12 which consists of a refractory-metal silicide is formed.
At this time, the thickness of the 1st oxide film 5, the nitride 6, the 2nd oxide film 7, especially the nitride 6 needs to be set up so that it may reach 1st gate electrode 3 and the refractory-metal silicide layer on the 2nd gate electrode 8 may carry out a bridging. After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 1 will be completed.

[0026] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 1 , and a final nonvolatile memory cell is completed.

[0027] According to the 1st embodiment form of this invention, since the 2nd gate electrode 8 was formed also in the upper part of the charge accumulation layer 4, the controllability of a threshold voltage improves.
In addition, the same effect is acquired, even if it is the case where it constitutes from a p type MOS transistor, although the 1st embodiment form of this invention explained the case where a memory cell was constituted from an n type MOS transistor.
Moreover, the memory cell has an LDD structure and it may be single drain structure or double drain structure.

[0028] (2nd embodiment form)
Next, the 2nd embodiment form of this invention is explained.

Fig. 10 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.
This memory cell consists of an n type MOS transistor.
With the memory cell structure of the non-volatile memory concerning the 2nd embodiment form of this invention, the 2nd gate insulator layer 14 is formed in the front face of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
And the charge accumulation layers 4a and 4b are formed at the ends of the 2nd gate insulator layer 14.
On the 2nd gate insulator layer 14 and charge accumulation layers 4a and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed on each surface of gate electrode 3 and n+ type diffusion layer 11.

[0029] The memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention has LDD structure which constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration.
And a gate insulator layer consists of three layer cascade screen consisting of 1st gate insulator layer 13 (lower layer), 2nd gate insulator layer 14 (interlayer), and of the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated to these two charge accumulation layers 4a and 4b, the store status being one of the four following status, namely
(1)the status that neither accumulation layer 4a nor 4b are accumulating electrons,
(2)the status that only charge accumulation layer 4a is accumulating the electron,
(3)the status that only charge accumulation layer 4b is accumulating the electron,
(4)the status that charge accumulation layers 4a and 4b are both accumulating the electron.
The amount of threshold change of potential according to the existence/non-existence of the electron held at these two charge accumulation layers 4a and 4b is made to correspond to storage information "00", "01", "10" and "11."
Moreover, with this memory cell structure, since the charge accumulation layers 4a and 4b are located in the upper part of a channel field edge, the threshold voltage of a channel field center section is decided only by impurity concentration of a channel field, and it does not depend for it on the store status of the electron of the charge accumulation layers 4a and 4b.
Therefore, the faulty deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and faulty deletion which originates by that cause, such as the poor leakage, a poor program, and poor read-out can not be produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and highly reliable nonvolatile semiconductor memory can be realized.
It is advisable for the charge accumulation layers 4a and 4b to consist of silicon nitride of high charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer or a polycrystal silicon layer, it can be manufactured cheaply.
If the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are furthermore constituted from a silicon nitride (Si3N4 layer) which has a dielectric constant of about 2 times the one of a silicon oxide (SiO2 layer), a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is about 4nm - 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion

thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection extraction operation is reduced, and not only micronization of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0030] Although n- type diffusion layer 10 is established for the purpose of the pressure-proof enhancement in a source field and a drain field and LDD structure is constituted from a memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention, a source field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4a-4b, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film which has a high dielectric constant is used for 2 gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved As a metal oxide film, there are TiO2, Ta2O5, aluminum2O5, and PZT and SBT.

[0031] Next, an operation of the non-volatile memory concerning the 2nd embodiment form of this invention is explained using the Fig. 11 and the Fig. 12 .
Fig. 11 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 12 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 11 , at the time of the writing of a memory cell, about 7-8V is impressed to gate G, about 5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field by the channel thermoelectron (CHE).
When pouring an electron into charge accumulation layer 4a by the side of a source field you just need to replace in the above-mentioned case the voltage impressed to each drain D and source S.
On the other hand, as shown in Fig. 12 , a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler-Nordheim (FN) type tunnel current.
Moreover, when the gate electrode 3 is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells.
In this case, source S and drain D should just take as the p type semiconductor substrate 1 and this potential.
Moreover, it is also possible to impress the right voltage different from the potential of the p type semiconductor substrate 1 to drain D, and to draw out an electron for source S only from floating potential (Floating), then charge accumulation layer 4a by the side of drain D.
What is necessary is to impress a right voltage to source S, in drawing out an electron only from charge accumulation layer 4b by the side of source S, and just to let drain D be floating potential.

[0032] The writing of a memory cell can also be performed like a deletion of a memory cell using FN current.
About 10V is impressed between gate G and the p type semiconductor substrate 1, and an electron is poured into the charge accumulation layers 4a and 4b with FN current.
In this case, an electron can be simultaneously poured into two or more memory cells in which have gate G in common.

[0033] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be

memorized in one cell.

[0034] Next, the manufacture technique of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention is explained using Fig. 13 through Fig. 19 .
As first shown in Fig. 13 , the small silicon nitride of charge store capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed.
Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD (Jet-Vapor-Deposition) method.
The JVD method is indicated by bibliography "T.P.Ma, IEEE Transactions ON Electron Devices, Volume 45 Number 3, and March 1998 p680."
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, the silicon nitride of small charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0035] Next, as shown in Fig. 14 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then the 1st gate insulator layer 13 of the front face of the p type semiconductor substrate 1 of the field which uses the gate electrode 3 as a mask and forms a source field and a drain field, the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 are dry-etched self-conformably.

[0036] Next, as shown in Fig. 15 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 2nd embodiment form of this invention, since it reaches 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which contains HF gas, instead of the wet etching method which used the etching reagent.

[0037] Next, as shown in Fig. 16 , it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the silicon nitride 18 of high charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
And as shown in Fig. 17 , anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layers 4a and 4b which consisted of a silicon nitride of high charge store capacity are formed.

[0038] Next, as shown in Fig. 18 , after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
N- type diffusion layer 10 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0039] Next, as shown in Fig. 19 , after forming the side wall spacer 9 in the side wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
N+ type diffusion layer 11 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 and the side wall spacer 9 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0040] Next, membranes of high-melting point metals such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, and then, by heat-treating the p type semiconductor substrate 1 in an inert atmosphere, in each front face of the gate electrode 3 and n+ type diffusion layer 11 the electric conduction layer 12 which consists of a refractory-metal silicide is formed.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 10 will be completed.

[0041] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 10 , and a final nonvolatile memory cell is completed.

[0042] Thus, with the 2nd embodiment form of this invention, the charge accumulation layers 4a and 4b can be formed in a self-matching way down the ends of the gate electrode 3.
Therefore, micronization in the orientation of gate length of a cell transistor is attained.
Thereby, large capacity and high-density nonvolatile semiconductor memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and nonvolatile semiconductor memory reduced sharply can be realized.

[0043] Moreover, the width of face of the orientation of channel length of the charge accumulation layers 4a and 4b can be easily controlled by adjustment of the etch-rate difference and etching time of the 1st gate insulator layer 13, and of the 3rd gate insulator layer 15 and the 2nd gate insulator layer 14,.
Thereby, the charge accumulation layers 4a and 4b can be arranged symmetrically.
And since the charge accumulation layers 4a and 4b are electrically separated completely by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b do not happen.
Furthermore, since the charge accumulation layers 4a and 4b are insulated completely from a source field, a drain field, the gate electrode 3, and a channel field by the 1st insulator layer 13, 3rd insulator layer 15, and oxide film 16, the nonvolatile semiconductor memory with excellent charge hold property can be offered.
Charge accumulation layers 4a and 4b are formed extending in the orientation of a channel field from the edge of the gate electrode 3, and the current-conducting characteristics of a memory cell are mainly set by the charge store status of the part by the side of the channel field of the charge accumulation layers 4a and 4b.
Therefore, if the length of the orientation of gate length of this part is reduced to the limits, more detailed nonvolatile semiconductor memory can be offered.

[0044] Furthermore, since the cellular structure is easily realizable at usual CMOS process, nonvolatile semiconductor memory can be manufactured at low cost using the existing production line.

[0045] (3rd Embodiment Form) Next, the 3rd embodiment form of this invention is explained.
The 3rd embodiment form of this invention is the 2nd embodiment form shown in Fig. 10 with the silicon oxide transposed for the 1st gate insulator layer 13 and the 2nd gate insulator layer 14 are transposed to a silicon nitride, and the 3rd gate insulator layer 15 is to a silicon oxide.
Hereafter, the manufacture technique of the memory cell of the nonvolatile semiconductor memory concerning the 3rd embodiment form of this invention is explained with reference to Fig. 13 through Fig. 15.

[0046] First, as for the memory cell of the nonvolatile semiconductor memory concerning the 3rd embodiment form of this invention, the p type semiconductor substrate 1 is oxidized thermally, and the 1st gate insulator layer 13 which consists of an about 10nm silicon oxide is formed.

After 1st gate insulator layer 13 formation, the silicon nitride of the low charge store capacity is deposited by the JVD method and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, a silicon oxide is deposited by CVD and the about 10nm 3rd gate insulator layer 15 is formed (refer to the Fig. 13).

[0047] Next, after depositing the about 50-250nm polycrystal silicon layer which is doped with n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then, at the 1st gate insulator layer 13, the 2nd gate insulator layer 14, and the 3rd gate insulator layer 15 of the front face of the p type semiconductor substrate 1 of the field which forms a source field and a drain field using the gate electrode 3 as a mask, dry etching is carried out self-adjustingly (refer to the Fig. 14).

[0048] Next, the p type semiconductor substrate 1 is oxidized thermally, and a thin silicon oxide is formed all over p type semiconductor substrate 1.
Then, the space 17 for charge accumulation layer formation is formed.
The space 17 for this charge accumulation layer formation is formed by using the etching reagent with the large etch rate on the 2nd gate insulator layer 14 rather than on the1st gate oxide-film 13 and the 3rd gate insulator layer 15, and carrying out wet etching selectively the edge of the 2nd gate insulator layer 14.
With the 3rd embodiment form of this invention, since 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon oxide and the 2nd gate insulator layer 14 is constituted from a silicon nitride, for example a phosphoric-acid type may be used as an etching reagent.
In addition, since the silicon nitride 14 hardly oxidizes by thermal oxidation processing, an oxide film is not formed in the side face of the 2nd gate insulator layer, but, for this reason, the selectivity of etching improves (refer to the Fig. 15).
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which contains CF4 gas instead of the wet etching method which used the etching reagent.
The subsequent process is the same as the 2nd embodiment form.

[0049] (4th embodiment form) Next, the 4th embodiment form of this invention is explained. Fig. 20 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.
The 4th embodiment form of this invention is the example that constituted the memory cell from a p type MOS transistor.
As shown in Fig. 20, with the memory cell structure of the non-volatile memory concerning the 4th embodiment form of this invention, the 2nd gate insulator layer 14 is formed in the surface of the n-type-semiconductor substrate 19 through the 1st gate insulator layer 13.
The charge accumulation layers 4a and 4b are formed in the ends of 2 gate insulator layer 14.
On the 2nd gate insulator layer 14 and charge accumulation layer 4a and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and p- type diffusion layer 20 of the low impurity concentration which touches a channel field, and p+ type diffusion layer 21 of the high impurity concentration located in the outside of this p-type diffusion layer 20 are formed in the n-type-semiconductor substrate 19 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and p+ type diffusion layer 21.

[0050] Next, an operation of the non-volatile memory concerning the 4th embodiment form of this invention is explained using the Fig. 21 and the Fig. 22 .
Fig. 21 is a cross section of the non-volatile memory explaining a write-in operation.

Fig. 22 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 21 , at the time of the writing of a memory cell, about 5V is impressed to gate G, and about -5V is impressed to drain D, respectively, and let source S be floating potential.
Thus, a voltage is impressed, energy is given the electron of the tunnel phenomenon reason between band-bands by the electric field near the drain field, and an electron is poured into charge accumulation layer 4b by the side of a drain field.
The voltage impressed to drain D and source S is replaced with each other, in pouring an electron into charge accumulation layer 4a by the side of a source field.
On the other hand, as shown in Fig. 22, a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by Fig. out an electron from the charge accumulation layers 4a and 4b using FN current.
Moreover, when gate G is shared with plural cells, an electron can be simultaneously drawn out from those memory cells.
In this case, source S and drain D are taken as the n-type-semiconductor substrate 19, this potential, or floating potential.

[0051] It is possible to perform it, even if the writing of a memory cell uses a channel thermoelectron like the 2nd embodiment form of this invention.
In this case, about -2.5V is impressed to gate G, about -5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field by the channel thermoelectron.
On the other hand, just to replace the voltage impressed to drain D and source S is replaced with each other, in pouring an electron into charge accumulation layer 4a of a source field.

[0052] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current that flows between source S and drain D.
It uses that the current transfer characteristics near the source field and the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0053] (5th embodiment form) Next, the 5th embodiment form of this invention is explained.
Generally, a peripheral circuit is arranged in semiconductor memory around a memory cell array.
For example, there are a decoder, writing/deletion circuit, a readout circuitry, an analog circuit, various kinds of I/O circuits, various kinds of capacitor circuits, etc. as the peripheral circuit.
The 5th embodiment form of this invention shows the example that manufactures simultaneously the MOS transistor which constitutes these peripherals circuit using the manufacturing process of the memory cell transistor of the 2nd - the 4th embodiment form.
Fig. 23 is a cross section showing the structure of the MOS transistor that constitutes the peripheral circuit of the nonvolatile semiconductor memory concerning the 5th embodiment form of this invention.
As shown in Fig. 23 , according to the 5th embodiment form of this invention, seven kinds of MOS transistors (Tr1-Tr7) from which a gate insulator layer is different in addition to a memory cell transistor (memory cell Tr) are realizable.
In addition, the memory cell transistor of Fig. 23 is a memory cell transistor shown in Fig. 10.
Moreover, MOS transistors Tr1-Tr7 show n type MOS transistor altogether. n- type diffusion layer 10 of a memory cell transistor and n+ type diffusion layer 11, and the electric conduction layer 12 are omitted in order to make a drawing legible.
MOS transistors Tr1-Tr7 are omitted in the same way.

[0054] Next, the manufacture technique of an MOS transistor shown in Fig. 23 is explained using

the Fig. 24 or the Fig. 30.
As shown in Fig. 24 , the small silicon nitride of charge store capacity is deposited by the JVD method all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed.
Well-known exposure technique and well-known dry etching technique remove the 1st gate insulator layer 13 of the field of the part on the p type semiconductor substrate 1 after 1st gate insulator layer 13 formation.
And as shown in Fig. 25, a silicon oxide is deposited by CVD and the about 5-10nm 2nd gate insulator layer 14 is formed.
Exposure technique and dry etching technique remove the 2nd gate insulator layer 14 of a part of field after 2nd gate insulator layer 14 formation.
Then, as shown in Fig. 26 , the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.
Exposure technique and dry etching technique remove the 3rd gate insulator layer 15 of a part of field after 3rd gate insulator layer 15 formation.
It does in this way and the 1st gate insulator layer 13 and seven kinds of gate insulator layers which reach 2nd gate insulator layer 14 and consist of at least one of the 3rd gate insulator layers 15 are realized.
In the above method, seven kinds of gate insulator layers are realized

[0055] Next, as shown in Fig. 27 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and plural gate electrodes 3 are formed.
Furthermore, the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and 3 gate insulator layer 15 of the surface of the p type semiconductor substrate 1 in the field which uses the gate electrode 3 as a mask and forms each source field and drain field of a memory cell transistor and an MOS transistor by dry etching, is removed.

[0056] Next, as shown in Fig. 28, the field which forms MOS transistors Tr1-Tr7 is covered by the photoresist 22, and wet etching of the field which forms a memory cell transistor is carried out.
An etching reagent uses what has an etching speed of the 2nd gate insulation film 14 quicker than the 1st gate oxidization film 13 and the 3rd gate insulation film 15.
The edge of the 2nd gate insulation film 14 of the domain that forms a memory cell transistor by this wet etching is etched alternatively, and the space 17 for electric charge accumulation layer formation is formed.
Since the 1st gate oxide film 13 and the 3rd gate insulator layer 15 are constituted from a silicone nitriding film and the 2nd gate insulation layer 14 is constituted from a silicone oxide film, for example, a fluoric acid type is used as etching reagent.
And as shown in Fig. 29, it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
Then, as shown in Fig. 30, anisotropic etching by RIE is performed to the whole surface of p type semiconductor substrate 1, and the electric charge accumulation layers 4a and 4b that consisted of high silicone nitriding films of electric charge accumulation capability are formed in the domain that forms a memory cell transistor.

[0057] According to the 5th embodiment form of this invention, seven kinds of MOS transistors Tr1-Tr7 that have the gate insulator layer with which film thickness differs can be manufactured simultaneously with a memory cell transistor.
Thereby, the MOS transistor corresponding to operating voltage various from the high pressure-proofing transistor of a high-voltage operation to a super-low voltage operation transistor can be offered.
Furthermore, it is possible to realize an n type MOS transistor and a p type MOS transistor.
Moreover, the gate electrode 3 of a memory cell transistor and MOS transistors Tr1-Tr7 consists of the same material, and is formed at the same exposure process and a dry etching process.

Therefore, it is possible to offer a detailed transistor with few position doubling gaps of a photo mask.

[0058] (6th embodiment form) Next, the 6th embodiment form of this invention is explained.
In the form of this 6th embodiment form, the example that realizes electrically the volatile memory in which writing and read-out are possible on the same tip at the non-volatility memory that can be written in and eliminated, and high speed is shown.
Fig. 31 is a sectional view showing the memory cell structure of the nonvolatile memory carried in the semiconductor memory storage concerning the 6th embodiment form of this invention.
Fig. 32 is a sectional view showing the memory cell structure of the volatile memory carried in starting-6th case of the operation of this invention semiconductor memory storage.
Non-volatile memory of Fig. 31 and volatile memory of Fig. 32 are loaded together on the same chip.

[0059] (A) As shown in non-volatile memory Fig. 31, the memory cell of the non-volatile memory concerning the 6th embodiment form consists of an n type MOS transistor.
And with the memory cell structure of this non-volatile memory, the 2nd gate insulator layer 14 is formed through the 1st gate insulator layer 13 on the principal plane of the p type semiconductor substrate 1.
The charge accumulation layer 4 (4a, 4b) is formed in the both ends of the 2nd gate insulator layer 14.
On the 2nd gate insulator layer 14 and the charge accumulation layer 4, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of gate electrode 3 and n+ type diffusion layer 11.

[0060] The memory cell of the non-volatile memory concerning the 6th embodiment form of this invention has LDD structure that constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration and an n+ type diffusion layer 11 of high impurity concentration.
And it consists of a three layer laminating films by which a gate insulator layer consists of the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer), and the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layer 4 (4a, 4b) is formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated in these two electric charge accumulation layers 4a and 4b, and the accumulation state can take the following four states.

(1) Neither of the electric charge accumulation layers 4a and 4b is accumulating the electron.
(2) Only electric charge accumulation layer 4a is accumulating the electron.
(3) Only electric charge accumulation layer 4b is accumulating the electron.
(4) The electric charge accumulation layers 4a and 4b are accumulating the electron.

The amount of change of the threshold voltage produced by the existence of the electron held at these two electric charge accumulation layers 4a and 4b is made to correspond to memory information "00", "01", "10" and "11".
Moreover, with this memory cell structure, since the charge accumulation layer 4 is located in the upper part of a channel field edge, the threshold voltage of the central part of a channel field is decided only by impurity concentration of a channel field, and it does not depend for it on the accumulation state of the electron of the charge accumulation layer 4.
Therefore, fault deletion (over-erase) by the excess and deficiency of the electron of the electric charge accumulation layer 4 is prevented, and the poor leakage resulting, a poor program, and poor read-out from fault deletion must have been produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only

by the gate voltage, and can realize highly reliable non-volatile memory.
What is necessary is for the charge accumulation layer 4 just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge holds property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0061] Although LDD structure is constituted from a memory cell of a nonvolatile memory by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4a and 4b, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film that has a high dielectric constant is used for 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
For example, it is possible to use TiO2, Ta 2O5, Al2O5, PZT and SBT as a metal oxide film.

[0062] Next, an operation of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention is explained using Fig.. 33 and Fig. 34 .
Fig. 33 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 34 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 33, at the time of the writing of a memory cell, about 7-8V is impressed to gate G, about 5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b of a drain field by the channel thermo electron (CHE).
What is necessary is just to replace the voltage impressed to each of drain and Sauce S, in pouring an electron into electric charge accumulation layer 4b of a sauce field.
On the other hand, as shown in Fig. 34, a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when plural memory cells share gate G, an electron can be simultaneously drawn out from those memory cells.
In this case, what is necessary is just to make Sauce S and drain D into the same potential as p type semiconductor substrate 1.
Moreover, if different right voltage from the potential of p type semiconductor substrate 1 is impressed to drain electrode and sauce electrode is made into floating potential (Floating), it is also possible to draw out an electron only from electric charge accumulation layer 4b of drain electrode.
What is necessary is to impress right voltage to sauce electrode, in drawing out an electron only from electric charge accumulation layer 4a of sauce electrode, and just to let drain electrode be floating potential.

[0063] The writing of a memory cell can also be performed like a deletion of a memory cell using FN current.
About 10V is impressed between gate G and the p type semiconductor substrate 1, and an

electron is poured into the charge accumulation layers 4a and 4b with FN current.
In this case, an electron can be simultaneously poured into plural memory cells in which gate G is common.

[0064] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current that flows between source S and drain D.
It uses that the current transfer characteristics near a source field and the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
The information for 2 bits is memorizable in one cell by acquiring the four different current transfer characteristics according to four accumulation states of the electric charge accumulation layers 4a and 4b.

[0065] (B) As shown in volatile-memory Fig. 32, the memory cell of the volatile memory concerning the 6th embodiment form of this invention consists of an n type MOS transistor.
With the memory cell structure of this volatile memory, the 2nd gate insulator layer 14 of Fig. 31 is directly arranged on the principal plane of the p type semiconductor substrate 1.
And although the charge accumulation layer 4 (4c, 4d) is formed in the both ends of the 2nd gate insulator layer 14 like the non-volatile memory of Fig. 31, it differs from the non-volatile memory of Fig. 31 in that these charge accumulation layers 4c and 4d are arranged on the principal plane of p type semiconductor substrate 1 through the tunnel insulation layer 23.
On the 2nd gate insulator layer 14 and the charge accumulation layer 4, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of gate electrode 3 and n+ type diffusion layer 11.

[0066] The memory cell of the volatile memory concerning the 6th embodiment form of this invention has LDD structure that constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration and an n+ type diffusion layer 11 of high impurity concentration.
And a gate insulator layer consists of the 2nd gate insulator layer 14, a tunnel insulator layer 23 and the 3rd gate insulator layer 15, and the charge accumulation layer 4 is formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated in these two electric charge accumulation layers 4c and 4d, and the accumulation state can take the following four states.

(1) Electric charge accumulation layers 4c and 4d neither is accumulating the electron.
(2) Only electric charge accumulation layer 4c is accumulating the electron.
(3) Only 4d of electric charge accumulation layers is accumulating the electron.
(4) The electric charge accumulation layers 4c and 4d are accumulating the electron.

The amount of which is produced by the existence of the electron held at these two charge accumulation layers 4c and 4d threshold change of potential is made to correspond to a storage information "00", "01", "10" and "11".
Moreover, with this memory cell structure, since the charge accumulation layer 4 is located in the upper part of the edge of a channel field, the threshold voltage of the central part of the channel field is decided only by impurity concentration of a channel field, and it does not depend for it on the accumulation state of the electron of the charge accumulation layer 4.
Therefore, the fault deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layer 4 is prevented, and the poor leakage, a poor program, and poor read-out which originates in a fault deletion by that cause must have been produced.

Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and can realize highly reliable volatile memory.
What is necessary is for the charge accumulation layer 4 just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
Furthermore, if the 3rd gate insulator layer 15 is constituted from a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm to about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0067] Although LDD structure is constituted from a memory cell of a nonvolatile memory by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4c and 4d, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film that has a high dielectric constant is used for 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
For example, it is possible to use TiO2, Ta 2O5, Al2O5, PZT and SBT as a metal oxide film.

[0068] In the volatile memory concerning the 6th embodiment form of this invention, the tunnel insulator layer 23 is arranged in the lower part of a charge accumulation layers 4c and 4d.
The tunnel insulator layer 23 consists of a silicon oxide of the thin film which has the thickness in which direct tunneling is possible, and makes possible high-speed read-out and write-in in 100ns or less required of a dynamic RAM.
When the tunnel insulator layer 23 is constituted from a silicon oxide, the thickness is just 3nm or less.
Moreover, if the tunnel insulator layer 23 is constituted from a silicon nitride 3nm or less, a silicon-oxide conversion thickness can realize stably the very thin gate insulator layer which is about 1.5nm.
Since the electron accumulated by the leakage current through the tunnel insulator layer 23 at the charge accumulation layer 4 decreases gradually, prolonged data-hold is difficult in practice. However, re-writing is possible enough within the refreshment term of a usual dynamic RAM, and it is thought that it is satisfactory at all in the operation as a dynamic RAM.
This is shown in 1995 IEDM digest p.867 by C.H-J.Wann et al.

[0069] Reading of a memory cell is performed by detecting the read-out current which flows between a source electrode and drain electrodes.
It uses that the current transfer characteristics near a source field and the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4c and 4d.
To which a bias shall be carried out between source electrode and drain electrode should just choose the direction where the modulation of current transfer characteristics appears notably.
The information for 2 bits is memorizable in one cell by acquiring the four different current transfer characteristics according to four accumulation states of the electric charge accumulation layers 4c and 4d.

[0070] Furthermore, if the volatile memory concerning the 6th embodiment form of this invention does not pour a charge into the charge accumulation layers 4c and 4d, it is possible to make it operate as a usual MOS transistor.

[0071] (C) The manufacture method of a non-volatility and a volatile mixed-loading memory
Next, the manufacture method of the memory cell of the nonvolatile memory concerning the 6th embodiment form of this invention and an volatile memory is explained using Fig. 35 to Fig. 43 and using Fig. 44 to Fig. 52.
Fig. 35 to Fig. 43 are showing the manufacture method of the non-volatile memory concerning the 6th embodiment form of this invention.
Fig. 44 to Fig. 52 are showing the manufacture method of the volatile memory concerning the 6th embodiment form of this invention.

[0072] As first shown in Fig. 35 and Fig. 44, the small silicon nitride of charge store capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed.
After 1st gate insulator layer 13 formation, the non-volatile memory formation field of Fig. 35 is covered by the photoresist for example and only the 1st gate insulator layer 13 of the volatile-memory formation field of Fig. 44 is removed by the wet etching method for example, using the heating phosphoric-acid solution.
Therefore, the 1st gate insulator layer 13 is formed only in the non-volatile memory formation field of Fig. 35.
Deposition of a silicone nitriding film with small electric charge accumulation capability is performed for example, by the JVD method.

[0073] Next, as shown in the Fig. 36 and the Fig. 45 , a silicon oxide is deposited all over p type semiconductor substrate 1 by CVD, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, a silicone nitriding film with small electric charge accumulation capability is deposited by the JVD method, and the about 10nm 3rd gate insulation film 15 is formed.
After all, the 1st, the 2nd and 3rd gate insulator layers 13, 14 and 15 are formed in the non-volatile memory formation field of Fig. 36, and the 2nd and the 3 gate insulator layers 14 and 15 are formed in the volatile-memory formation field of Fig. 45.

[0074] Next, as shown in the Fig. 37 and the Fig. 46 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then, in the nonvolatile memory formation field of Fig. 37, dry etching the 1st gate insulation film 13, the 2nd gate insulation film 14 and the 3rd gate insulation film 15 on the surface of p type semiconductor substrate 1 of the field which forms a sauce filed and a drain field is carried out self-adjustingly.
On the other hand, in the volatile-memory formation field of Fig. 46 , dry etching of the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 is carried out self-adjustingly.

[0075] Next, as shown in the Fig. 38 and the Fig. 47, the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by carrying out wet etching of the end of the 2nd gate insulator layer 14 alternatively using etching liquid with an etching speed of the 2nd gate insulation film 14 quicker than the 1st gate oxide-film 13.
The space 17 to form a charge accumulation layer in the non-volatile memory formation field in the nonvolatile memory formation domain of Fig. 38 and the space 17 to form a charge accumulation layer in the volatile memory formation field in the nonvolatile memory formation domain of Fig. 47 is formed simultaneously.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 6th embodiment form of this invention, since the 1st gate oxide-film 13 and the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from

a silicon oxide.
Moreover, you may form this space 17 by the plasma dry etching method using the gas which contains HF gas instead of the wet etching method which used etching reagent.

[0076] Next, as shown in the Fig. 39 and the Fig. 48 , it oxidizes by the RTO method and the tunnel insulator layer 23 which consists of the silicon oxide in which a direct tunnel is possible is formed for the whole surface of p type semiconductor substrate 1.

[0077] Next, as shown in the Fig. 40 and the Fig. 49 , it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
And as shown in the Fig. 41 and the Fig. 50 , anisotropic etching by RIE is performed to whole surface of the p type semiconductor substrate 1, and the charge accumulation layer 4 (4a, 4b, 4c, 4d) which consisted of a silicon nitride of high charge store capacity is formed simultaneously.

[0078] Next, as shown in the Fig. 42 and the Fig. 51 , after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
It forms by activating the impurity which n- type diffusion layer 10 used the gate electrode 3 as the mask with ion-implantation technique, poured in n type impurity, and was poured in with subsequent heat treatment.

[0079] Next, as shown in the Fig. 43 and the Fig. 52 , after forming the side wall spacer 9 in the side attachment wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
It forms by activating the impurity which n+ type diffusion layer 11 used the gate electrode 3 and the side wall spacer 9 as the mask with ion-implantation technique, poured in n type impurity, and was poured in with subsequent heat treatment.

[0080] And the thing for which high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere and the electric conduction layer 12 which consists of a refractory-metal silicide is formed in each surface of the gate electrode 3 and n+ type diffusion layer 11.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure of volatile memory shown in the non-volatile memory the Fig. 32 and having shown in Fig. 31 will be completed.

[0081] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of the Fig. 31 and the Fig. 32 , and the semiconductor device which carried final non-volatile memory and final volatile memory is completed.

[0082] Thus, with the 6th embodiment form of this invention, the charge accumulation layer 4 (4a, 4b, 4c, 4d) can be formed in a self-matching target down the ends of the gate electrode 3.
Therefore, micronization of the orientation of gate length of the memory cell transistor of the Fig. 31 and the Fig. 32 is attained.
Thereby, large capacity, high-density non-volatile memory, and volatile memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and the non-volatile memory and volatile memory that were reduced sharply can be realized.

[0083] The width of the direction of channel length of the charge accumulation layer 4 is easily controllable by the etching speed difference of p type semiconductor substrate 1, the 1st gate insulation film 13, the 3rd gate insulation film 15, and the 2nd gate insulation film 14, and regulation of etching time.

Thereby, the charge accumulation layer 4 can be arranged symmetrically.
And since it is electrically separated completely by the 2nd gate insulation film 14 between the electric charge accumulation layers 4, the interaction between the electric charge accumulation layers 4 does not happen.
Furthermore, from a source field, a drain field, the gate electrode 3, and a channel field, since the 1st insulator layer 13, tunnel insulator layer 23, 3rd insulator layer 15, and oxide film 16 insulate completely, the charge accumulation layer 4 can offer the non-volatile memory and volatile memory which were excellent in the charge hold property.
The charge accumulation layer 4 is extended and formed in the direction of a channel field from the end of gate electrode 3, and the current transfer-characteristics of a memory cell is mostly decided by the electric change accumulation state of the fraction by the side of the channel field of the electric charge accumulation layer 4.
Therefore, if the length of the orientation of gate length of this fraction is reduced to a limitation, more detailed non-volatile memory and more detailed volatile memory can be offered.

[0084] Since it is easily realizable at usual CMOS process, the cellular structure can manufacture non-volatile memory and volatile memory by the low cost using the existing production line.

[0085] Furthermore, since the greater part of the manufacturing process is communalized, it is a low cost, and above-mentioned non-volatile memory and above-mentioned volatile memory are the short manufacture time necessary for completion, and can manufacture the semiconductor device consolidated with non-volatile memory and volatile memory.

[0086] In addition, although the 1st gate insulator layer 13 is constituted from silicon nitride and the 2nd gate insulator layer 14 are constituted from a silicon oxide and the 3rd gate insulator layer 15 is constituted from silicon nitride in the 6th embodiment form of this invention, you may constitute the 1st gate insulator layer 13 from a silicon oxide, the 2nd gate insulator layer 14 from a silicon nitride, and the 3rd gate insulator layer 15 from a silicon oxide.
In this case, for example, the 1st gate insulator layer 13 consists of an about 10nm silicon oxide which oxidized thermally the p type semiconductor substrate 1.
The 2nd gate insulator layer 14 consists of a low silicon nitride of the about 5-10nm-charge store capacity deposited by the JVD method.
The 3rd gate insulator layer 15 consist of an about 10nm silicon oxide deposited by CVD.
Moreover, since formation of the space 17 for charge accumulation layer formation constitutes 1st gate oxide-film 13 and constitutes the 3rd gate insulator layer 15 from a silicon oxide and constitutes the 2nd gate insulator layer 14 from a silicon nitride, it should just use for example, a phosphoric-acid type as an etching reagent.

[0087](7th Embodiment Form) Next, the 7th embodiment form of this invention is explained.
The 7th embodiment form shows the example which realizes the non-volatility memory which can be written in and eliminated electrically, and the volatile memory in which writing and read-out at high speed are possible on the same chip like the 6th embodiment form of the above.
Fig. 53 is a cross section showing the memory cell structure of the nonvolatile memory carried in the semiconductor memory storage concerning the 7th embodiment form of this invention.
Fig. 54 is a cross section showing the memory cell structure of the volatile memory carried in the semiconductor memory storage concerning the 7th embodiment form of this invention.
Non-volatile memory of Fig. 53 and volatile memory of Fig. 54 are consolidated on the same chip.
Since it is the same as that of the 6th embodiment form of the above about the non-volatile memory shown in Fig. 53, the explanation is omitted.

[0088] As shown in Fig. 54, the memory cell of the volatile memory concerning the 7th embodiment form of this invention consists of an n type MOS transistor.
And with the memory cell structure of this volatile memory, charge accumulation layer 4e is arranged through the tunnel insulator layer 23 on the principal plane of the p type semiconductor substrate 1.

On charge accumulation layer 4e, the gate electrode 3 is formed through the 4th gate insulator layer 24.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and n+ type diffusion layer 11.

[0089] The memory cell of the volatile memory concerning the 7th embodiment form of this invention has LDD structure that constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration.
And it consists of a laminated structure to which a gate insulator layer changes from the tunnel insulator layer 23 and the 4th gate insulator layer 21, and charge accumulation layer 4e is arranged between the tunnel insulator layer 23 and the 4th gate insulator layer 24.
An electron is accumulated to this charge accumulation layer 4e, and the amount of the threshold voltage produced by the existence of the electron held at this electric charge accumulation layer 4e is made to correspond to memory information "0" and "1".
What is necessary is for charge accumulation layer 4e just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge holds property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
If the 4th gate insulator layer 24 is furthermore constituted from a silicon nitride (Si_3N_4 layer) which has an about 2 times of a silicon oxide (SiO_2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm to about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out.
Therefore, voltage at the time of electronic pouring operation and extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0090] Although LDD structure is constituted from a memory cell of a volatile memory by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.

[0091] In the volatile memory concerning the 7th embodiment form of this invention, the tunnel insulator layer 23 is arranged in the lower part of charge accumulation layer 4e.
The tunnel insulator layer 23 consists of a silicon oxide of the thin film which has the thickness in which direct tunneling is possible, and read-out write-in high-speed of it in 100 or less ns required of a dynamic RAM becomes possible.
When the tunnel insulator layer 23 is constituted from a silicon oxide, the thickness is just 3nm or less.
Moreover, if constituted from a silicon nitride 3nm or less, a silicon-oxide conversion thickness can stabilize for it and realize the very thin tunnel insulator layer 23 which is about 1.5nm.

[0092] Furthermore, if an electric charge is not poured into electric charge accumulation layer 4e, it is possible to also make it operate as a usual MOS transistor as for the volatile memory concerning the 7th embodiment form of this invention.

[0093] Next, the manufacture technique of the memory cell of the non-volatile memory and volatile memory concerning the 7th embodiment form of this invention is explained using Fig. 55 to Fig. 62, and Fig. 63 to Fig. 70 .
Fig. 55 to Fig. 62 is a cross section showing the manufacture method of the nonvolatile memory concerning the form of implementation of the 7th of this invention.
Fig. 63 to Fig. 70 is a cross section showing the manufacture method of the volatile memory concerning the 7th embodiment form of this invention.

[0094] As first shown in Fig. 55 and Fig. 63, the about 10nm 1st gate insulator layer 13 is formed by depositing the small silicon nitride of charge accumulation capability all over p type semiconductor substrate 1.
Deposition of the small silicon nitride of charge store capacity is performed by the JVD method, for example.
The about 5-10nm 2nd gate insulator layer 14 is formed by depositing a silicon oxide by the CVD method after 1st gate insulator layer 13 formation.
Then, the about 10nm 3rd gate insulator layer 15 is formed by depositing the small silicon nitride of charge accumulation capability by the JVD method.

[0095] Next, as shown in Fig. 56 and Fig. 64, after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, an gate electrode 3 is formed in the nonvolatile memory formation domain in Fig. 56 by carrying out patterning with exposure technnique and etching technnique.
Then dry etching of the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 on the surface of p type semiconductor substrate 1 of the field which forms a sauce field and a drain field by using gate electrode 3 as a mask is carried out self-adjustingly.
In the volatile memory formation field of Fig. 64, a ploycrystal silicone film, the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 are removed altogether, and the surface of p type semiconductor substrate 1 is exposed.

[0096] Next, as shown in Fig. 57, in a non-volatile memory formation field, the space 17 for charge accumulation layer formation is formed.
The space 17 for this charge accumulation layer formation is formed by carrying out wet etching of the end of the 2nd gate insulator layer 14 alternatively using etching liquid with an etching speed of the 2nd gate insulator layer 14 quicker than the 1st gate oxide-film 13 and the 3rd gate insulator layer 15.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 7th embodiment form of this invention, since it reaches 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
What is necessary is just to use for example, a fluoric acid type as etching reagent, since the 1st gate oxide-film 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the silicon oxide constitutes the 2nd gate insulator layer 14 in the 7th embodiment form of this invention.
Moreover, you may form the space 17 for charge accumulation layer system formation by the plasma dry etching method using the gas which changes to the wet etching method which contains HF gas instead of the wet etching method which used etching reagent.On the other hand, as shown in Fig. 65, in the volatile-memory formation field, the surface of the p type semiconductor substrate 1 has been exposed.

[0097] Next, as shown in Fig. 58 and Fig. 66, the tunnel insulator layer 23 which is by the RTO method for example, and consists of the silicon oxide which can be tunneled direct is formed all over p type semiconductor substrate 1.
After forming the tunnel insulation film 23, the silicon nitride 18 of high electric charge accumulation capability is deposited by the LPCVD method all over p type semiconductor substrate 1.

At this time, the space 17 for electric charge accumulation layer formation is completely embedded with the silicone nitriding film 18.
And as shown in Fig. 59, in a nonvolatile memory formation field, anisotropic etching by RIE is performed to the whole surface of p type semiconductor board 1, and the electric charge accumulation layer 4 (4a, 4b) which consisted of high silicon nitride 18 of electric charge accumulation capability is formed.
In that case, the volatile memory formation field shown in Fig. 67 is covered by photoresist, and the silicone nitride 18 is not etched.

[0098] After etching the silicon nitride 18, a silicon oxide is deposited all over p type semiconductor substrate 1, and the 4th gate insulator layer 24 is formed.
In this time the 4th gate insulator layer 24 of the nonvolatile memory formation field shown in Fig. 59 is removed.
The removal covers the volatile memory formation field shown in Fig. 67 by photoresist, and is performed by etching the 4th gate insulator layer 24 deposited on the nonvolatile memory formation field shown in Fig. 59.

[0099] Next, as shown in Fig. 68, the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method accumulates all over p type semiconductor substrate 1.
And patterning of the polycrystal silicon layer is carried out with exposure technique and etching technique, and gate electrode 3a is formed.
Then, using gate electrode 3a be an etching mask, dry etching of the tunnel insulator layer 23, electric charge accumulation layer 4e and the 4th gate insulator layer 24 on the surface of p type semiconductor substrate 1 of the field which forms a sauce field and a drain field is carried out self-adjustingly.
On the other hand, in a nonvolatile memory formation field, as shown in Fig. 60, all plycrystal silicone films may be removed, or patterning may be carried out according to gate electrode 3, and new gate electrode may be formed.

[0100] Next, as shown in the Fig. 61 and the Fig. 69 , after pouring in n type impurities by using the gate electrode 3 as a mask with ion implantation technique, n- type diffusion layer 10 is formed by activating the impurity poured in by heat treatment.

[0101] Next, as shown in the Fig. 62 and the Fig. 70 , after forming the side wall spacer 9 in the side wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
After pouring in n type impurity with ion implantation technique by using the gate electrode 3 and the sidewall spacer 9 as a mask, n+ type diffusion layer 11 is formed by activating the impurities poured in by heat treatment.

[0102] Next, high-melting point metal membranes, such as tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter method all over the p type semiconductor substrate 1 and the electric conduction layer 12 which consists of refractory metal silicide is formed on each surface of the gate electrode 3 and n+ type diffusion layer 11 by heat-treating p type semiconductor substrate 1 in an inactive atmosphere.
After the electric conduction layer 12 was formed, if the unreacted high-melting point metal which remained in fields other than the above is removed, the memory cell structure of a nonvolatile memory shown in Fig. 53 and of a volatile memory shown in Fig. 54 will be completed.

[0103] Although illustration is not carried out, after memory cell structure completion of Fig. 53 and Fig. 54, a final non-volatility memory cell and an volatile memory cell are completed through the usual CMOS manufacturing processes, such as an insulator-layer formation process between layers, a contact hole formation process, a wiring formation process and a passivation film formation process, one by one.

[0104] With the 7th embodiment form of this invention, although the 1st gate insulator layer 13 consists of silicon nitride, the 2nd gate insulator layer 14 consists of silicon oxide and the 3rd gate insulator layer 15 consists of silicon nitride, the 1st gate insulator layer 13 may be constituted from a silicon oxide, the 2nd gate insulator layer 14 may be constituted from a silicon nitride, and the 3rd gate insulator layer 15 be constituted from a silicon oxide.
In this case, for example, the 1st gate insulator layer 13 consists of an about 10nm silicon oxide which oxidized thermally the p type semiconductor substrate 1.
The 2nd gate insulator layer 14 consists of a low silicon nitride of the about 5-10nm charge store capacity deposited by the JVD method.
The 3rd gate insulator layer 15 consists of an about 10nm silicon oxide deposited by CVD.
Moreover, what is necessary is just to use for example, a phosphoric-acid type as an etching reagent in formation of the space 17 for electric charge accumulation layer formation, since the 1st gate oxide-film 13 and the 3rd gate insulator layer 15 are constituted from a silicon oxide and the 2nd gate insulator layer 14 is constituted from a silicon nitride.

[0105] Although both the memory cells of non-volatile memory and volatile memory explained the example which consists of an n type MOS transistor with the gestalt of the 6th and operation of the 7th of this invention, of course, you may be the memory cell of p type MOS transistor of an opposite conductivity type.
In this case, what is necessary is just to read the electric conduction type of a substrate or a diffusion layer as an opposite thing suitably in the above-mentioned explanation.

[0106] (8th Embodiment Form) Next, the 8th embodiment form of this invention is explained.
In the above 1st to the 7th embodiment forms, the structure of a charge accumulation layer is not directly contributed to the enhancement in electron-injection efficacy.
In the nonvolatile semiconductor memory of floating-gate structure, a stage is prepared in a channel fraction and the attempt which raises electron-injection efficacy is proposed. (S. Ogura and 1998 IEDM, p987, and the U.S. patent number of No. 5780341)
However, this proposal is weak to the defect and leak site in an oxidization film in order to adopt floating gate structure.
Moreover, there is a possibility that sufficient reliability cannot be acquired, also to the defect which may be generated at the time of stage structure formation.
The 8th embodiment form of this invention is an easy process, and can raise electron-injection efficacy.

[0107] Fig. 71 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.
This 8th embodiment form aims at enhancement in the electron-injection efficacy at the time of writing by the method of preparing a stage and an inclination in the channel field of a memory cell.
As shown in Fig. 71 , this memory cell consists of an n type MOS transistor.
And with the structure of the memory cell concerning the 8th embodiment form, the 2nd gate insulator layer 14 is formed on the surface of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
The charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14.
On the 2nd gate insulator layer 14 and charge accumulation layer 4a and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed on each surface of the gate electrode 3 and n+ type diffusion layer 11.

[0108] Furthermore, with the memory cell structure of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention, a stage 26 is formed in the channel field 25.
With this stage 26, the charge accumulation layer 4 will be located in the dispersion orientation of the electron in the p type semiconductor substrate 1.
Therefore, the injection efficiency of the electron at the time of writing improves.

[0109] The memory cell of the non-volatility semiconductor memory concerning the 8th embodiment form of this invention has the LDD structure where the sauce field and the drain field consisted of an n- type diffusion layer 10 of low impurities concentration and an n+ type diffusion layer 11 of high impurities concentration.
A gate insulator layer consists of three-layer laminating films which consist of the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer) and the 3rd gate insulator layer 15 (upper layer), and the electric charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated to these two charge accumulation layers 4a and 4b, and the accumulation state can take the following four status.
(1) The state where neither of the electric charge accumulation layers 4a and 4b is accumulating the electron,
(2) The state where only electric charge accumulation layer 4a is accumulating the electron,
(3) The state where only electric charge accumulation layer 4b is accumulating the electron,
(4) The state where the electric charge accumulation layers 4a and 4b are accumulating the electron,
The amount of which is produced by the existence of the electron held at these two charge accumulation layers 4a and 4b threshold change of potential is made to correspond to a storage information "00", "01", "10" and "11".
Moreover, with this memory cell structure, since the charge accumulation layers 4a and 4b are located in the upper part of a channel field edge, the threshold voltage of the central part of a channel field is decided only by impurity concentration of a channel field, and it does not depend for it on the accumulation state of the electron of the charge accumulation layers 4a and 4b.
Therefore, fault deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and the poor leakage, a poor program, and poor read-out resulting from fault deletion must have been produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and can realize highly reliable nonvolatile semiconductor memory.
What is necessary is for the charge accumulation layers 4a and 4b just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out.
Therefore, the voltage at the time of an electronic injection extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0110] Although LDD structure is constituted from a memory cell of a nonvolatile memory concerning the 8th embodiment form of this invention by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.

Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4a and 4b, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film that has a high dielectric constant is used for 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
For example, it is possible to use TiO2, Ta 2O5, Al2O5, PZT and SBT as a metal oxide film.

[0111] With the 8th embodiment form of this invention, although the stage 26 was formed in both of the source and a drain, you may prepare only in either.
Especially the memory that memorizes the information for 1 bit is enough if there is only one.

[0112] Next, an operation of the non-volatile memory concerning the 8th embodiment form of this invention is explained using Fig. 72 and Fig. 73.
Fig. 72 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 73 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 72 , at the time of the writing of a memory cell, about 6-8V is impressed to gate G, about 4-5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b of the drain field by the channel thermoelectron (CHE).
By having formed the stage 26 in the channel field 25, it is located in the electronic dispersion orientation at charge accumulation layer 4b.
For this reason, the electronic injection efficiency to charge accumulation layer 4b can improve, and improvement in the speed of an injection speed and reduction-ization of applied voltage can be attained.
What is necessary is just to replace with the above-mentioned case the voltage impressed to drain D and each source S, in pouring an electron into charge accumulation layer 4a of a source field.
On the other hand, as shown in Fig. 73 , a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when the gate electrode 3 is shared by plural memory cells, an electron can be simultaneously drawn out from those memory cells.
In this case, Sauce S and Drain D should just be taken as the same potential as p type semiconductor substrate 1.
Moreover, it is also possible to impress the right voltage different from the potential of the p type semiconductor substrate 1 to drain D, and to draw out an electron for source S only from floating potential (Floating), then charge accumulation layer 4a of drain D.
What is necessary is to impress a right voltage to source S, in drawing out an electron only from charge accumulation layer 4b of source S, and just to let drain D be floating potential.

[0113] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between source S and drain D.
It uses that the current transfer characteristics near the source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0114] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 8th embodiment form of this invention is explained using the Fig. 74 to the Fig. 82.
As first shown in Fig. 74, the wrap photoresist pattern 27 is formed for the field in which the channel field 25 is formed on the p type semiconductor substrate 1.
And as shown in Fig. 75, a stage 26 is formed by etching the p type semiconductor substrate 1

by the RIE method.

[0115] Next, as shown in Fig. 76, the small silicon nitride of charge store capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD method.
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0116] Next, as shown in Fig. 77, after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then dry etching of the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3rd gate Insulator layer 15 on the surface of p type semiconductor substrate 1 of the field which forms a sauce field and a drain field by using the gate electrode 3 as a mask is carried out self-adjustingly.

[0117] Next, as shown in Fig. 78 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 alternatively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14.
This space 17 is formed by carrying out wet etching of the end of the 2nd gate insulator layer 14 alternatively using etching liquid with an etching speed of the 2nd gate insulation film 14 quicker than the 1st gate oxide-film 13.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 8th embodiment form of this invention, since the 1st gate oxidization film 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which contains HF gas instead of the wet etching method which used the etching reagent.

[0118] Next, as shown in Fig. 79, it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
And as shown in Fig. 80, anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layers 4a and 4b which consisted of a silicon nitride of high charge store capacity are formed.

[0119] Next, as shown in Fig. 81 , after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
N- type diffusion layer 10 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0120] Next, as shown in Fig. 82, after forming the side wall spacer 9 in the side attachment wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
N+ type diffusion layer 11 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 and the side wall spacer 9 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0121] Next, membranes of high-melting point metals such as a tungsten, titanium, and cobalt,

are deposited by CVD or the spatter all over the p type semiconductor substrate 1, and then, by heat-treating the p type semiconductor substrate 1 in an inert atmosphere, in each front face of the gate electrode 3 and n+ type diffusion layer 11 the electric conduction layer 12 which consists of a refractory-metal silicide is formed.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 71 will be completed.

[0122] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 71 , and a final nonvolatile memory cell is completed.

[0123] Thus, with the 8th embodiment form of this invention, the charge accumulation layers 4a and 4b can be formed in a self-matching way down the ends of the gate electrode 3.
Therefore, micronization in the orientation of gate length of a cell transistor is attained.
Thereby, large capacity and high-density nonvolatile semiconductor memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and nonvolatile semiconductor memory reduced sharply can be realized.

[0124] Moreover, the width of face of the orientation of channel length of the charge accumulation layers 4a and 4b can be easily controlled by adjustment of the etch-rate difference and etching time of the 1st gate insulator layer 13, and of the 3rd gate insulator layer 15 and the 2nd gate insulator layer 14.
Thereby, the charge accumulation layers 4a and 4b can be arranged symmetrically.
And since the charge accumulation layers 4a and 4b are electrically separated completely by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b do not happen.
Furthermore, since the charge accumulation layers 4a and 4b are insulated completely from a source field, a drain field, the gate electrode 3, and a channel field by the 1st insulator layer 13, 3rd insulator layer 15, and oxide film 16, the nonvolatile semiconductor memory with excellent charge hold property can be offered.
Charge accumulation layers 4a and 4b are formed extending in the orientation of a channel field from the edge of the gate electrode 3, and the current-conducting characteristics of a memory cell are mainly set by the charge store status of the part by the side of the channel field of the charge accumulation layers 4a and 4b.
Therefore, if the length of the orientation of gate length of this part is reduced to the limits, more detailed nonvolatile semiconductor memory can be offered.

[0125] Furthermore, since the cellular structure is easily realizable at usual CMOS process, nonvolatile semiconductor memory can be manufactured at low cost using the existing production line.

[0126] And with the 8th embodiment form of this invention, the electron-injection efficacy at the time of writing can be raised.
For this reason, improvement in the speed of drawing speed and reduction-ization of the applied voltage at the time of writing can be attained.

[0127] (9th Embodiment Form) Next, the 9th embodiment of this invention is explained.
In the above 8th embodiment, the 9th embodiment of this invention makes unnecessary the 2nd insulator layer 14 arranged between charge accumulation layer 4a of Fig. 71 , and charge accumulation layer 4b, and has taken the configuration which made two charge accumulation layers 4a and 4b unify.
Fig. 83 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 9th embodiment of this invention. As shown in Fig. 83 , this memory cell

structure is arranged charge accumulation layers 4f instead of to the charge accumulation layers 4a and 4b and the 2nd insulator layer 14 of the 8th embodiment.

[0128] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 9th embodiment of this invention is explained using the Fig. 84 to the Fig. 89 .
Like the 8th embodiment, as shown in Fig. 84 , the photo resist pattern 27 is formed for the field in which the channel field 25 is formed on the p type semiconductor substrate 1.
And as shown in Fig. 85 , a level difference 26 is formed by etching the p type semiconductor substrate 1 by the RIE method.

[0129] Next, as shown in Fig. 86, the silicon nitride film of small charge store capacity is deposited all over p type semiconductor substrate 1, and the 1st gate insulator layer 13 having about 10nm is formed.
Deposition of the silicon nitride film of small charge store capacity is performed for example, by the JVD method.
The silicon nitrides film 18 high of charge store capacity is formed in about 5-10nm by the LPCVD method after 1st gate insulator layer 13 formation.
Then, the silicon nitride film of small charge store capacity is deposited by the JVD method, and the 3rd gate insulator layer 15 in about 10nm is formed.

[0130] Next, as shown in Fig. 87 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then, dry etching carried out conformably to the 1st gate insulator layer 13, the silicon nitride film 18 and the 3rd gate insulating film 15, of the surface of the p type semiconductor substrate 1 of the field, in which the source region, and drain region are formed using the gate electrode 3 as a mask, here, charge accumulation layers 4f is formed.

[0131] Next, as shown in Fig. 88, after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
Pouring n-type impurity with the gate electrode 3 as the mask with ion-implantation technique, then by activating the poured impurity with heat treatment, forms the n-type diffusion layer 10.

[0132] Next, as shown in Fig. 89, after forming the sidewall spacer 9 in the sidewall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
The n+ type diffusion layer 11is formed by pouring n type impurity using the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique and by activating the poured impurity by heat treatment.

[0133] Next, the high-melting point metal film, such as tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere, thereby forming the which consists of a refractory-metal silicide on the each surface of the gate electrode 3 and n+ type diffusion layer 11.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 83 will be completed.

[0134] In addition, although illustration is not shown, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 83 , and a final nonvolatile memory cell is completed.

[0135] (10th Embodiment Form) Next, the 10th embodiment of this invention is explained. Fig. 90

is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention.
In the above 8th and 9th embodiments, a level difference is prepared in the ends of a channel field by making a channel field into the concave status to a semiconductor substrate. In the 10th embodiment, a level difference is prepared in a channel field by making a channel field into the convex status to a semiconductor substrate.
And this 10th embodiment also aims at enhancement in the electron-injection luminous efficacy at the time of writing by preparing a level difference and an inclination in the channel field of a memory cell.

[0136] As shown in Fig. 90 , this memory cell consists of a p type MOS transistor. And in the structure of the memory cell concerning the 10th embodiment, the 2nd gate insulator layer 14 is formed in the surface of the n-type-semiconductor substrate 19 through the 1st gate insulator layer 13.
The charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14.
The gate electrode 3 is formed on the 2nd gate insulator layer 14 and charge accumulation layer 4a, and 4b through the 3rd gate insulator layer 15.
The sidewall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16.
The p- type diffusion layer 20 of the low impurity concentration which touches a channel field, and p+ type diffusion layer 21 of the high impurity concentration located in the outside of this p- type diffusion layer 20 are formed in the n-type-semiconductor substrate 19 of the lower part of this sidewall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and p+ type diffusion layer 21.

[0137] Furthermore, in the memory cell structure of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention, a level difference 26 is formed in the channel field 25.
Owing to this level difference 26, the charge accumulation layer 4 is located in the dispersion orientation of the electron in the p type semiconductor substrate 1. Therefore, the injection efficiency of the electron at the time of writing improves.

[0138] The memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention has LDD structure in which the source field and the drain field are constituted of a p- type diffusion layer 20 of low impurity concentration and a p+ type diffusion layer 21 of high impurity concentration.
And a gate insulator layer consists of a three-layered film, i.e. the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer) and the 3rd gate insulator layer 15 (upper layer). The charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated to these two charge accumulation layers 4a and 4b.
The state of accumulation can be four status:
(1) no electron is accumulated to charge accumulation layer 4a or 4b;
(2) the electron is accumulated to charge accumulation layer 4a only;
(3) the electron is accumulated to charge accumulation layer 4b only;
(4) the electron is accumulated to charge both accumulation layers 4a and 4b.
The amount of change of the threshold voltage which is produced by the existence of the electron held at these two charge accumulation layers 4a and 4b corresponds to the storage information "00", "01", "10", and "11".
Moreover, in this memory cell structure, since the charge accumulation layers 4a and 4b are located in the upper part of a channel field edge, the threshold voltage of the center of a channel field is decided only by impurity concentration of a channel field, and it does not depend on the accumulation status of the electron of the charge accumulation layers 4a and 4b.
Therefore, the fault deletion (over-erase) due to the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and the poor leakage, a poor program, and

poor read-out, which are caused in a fault deletion, never produced.
Moreover, only the gate voltage, thereby realizing highly reliable nonvolatile semiconductor memory, can suppress the leakage current between a source field and a drain field.
The charge accumulation layers 4a and 4b can be constituted of silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membranous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted of a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
If the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are furthermore constituted of a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) in dielectric constant, the very thin gate insulator layer which is 4nm - about 11nm in silicon-oxide conversion thickness can be stabilized.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection/extraction operation is lowered in battery, and not only a memory cell but also a circumference high-voltage operation element can be miniaturized.

[0139] Although p- type diffusion layer 20 is established for the purpose of the pressure-proof enhancement in a source field and a drain field and LDD structure is constituted from a memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention, a source field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layers 4a and 4b, it can consist of a silicon oxide, for example.
If the metal oxide film, which has a high dielectric constant, is used for the second gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
As a metal oxide film, there are TiO2, Ta2O5, aluminum2O5, and PZT and SBT.

[0140] In the 10th embodiment of this invention, the level difference 26 was formed in both by the side of the source and a drain, you may prepare only in either.
Especially the memory that memorizes the information for 1 bit is enough if there is only one side.

[0141] Next, an operation of the non-volatile memory concerning the 10th embodiment of this invention is explained using the Fig. 91 and the Fig. 92 .
Fig. 91 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 92 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 91, at the time of the writing of a memory cell, voltage of about 5V is impressed to gate G, and voltage of about -5V is impressed to drain D, respectively, and let source S be floating potential.
Thus, a voltage is impressed, energy is given the electron of the tunnel phenomenon reason between band-bands by the electric field near the drain, and it pours into charge accumulation layer 4b by the side of a drain field.
By having formed the level difference 26 in the channel field 25, charge accumulation layer 4b is located in the electronic injection orientation. For this reason, the electronic injection efficiency to charge accumulation layer 4b can improve, and improvement in the speed of an injection speed and reduction of applied voltage can be attained.
When pouring an electron into charge accumulation layer 4a by the side of a source, the voltage impressed to drain D and each source S is replaced with the above-mentioned case.
A memory cell is deleted by impressing a negative voltage (at least -5V) to gate G, as shown in Fig 92. and by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when two or more memory cells share the gate electrode 3, an electron can be simultaneously drawn out from those memory cells.

In this case, source S and drain D should just be taken as the n-type-semiconductor substrate 19 and this potential.
Moreover, if the right voltage different from the potential of the p type semiconductor substrate 1 is impressed to drain D and source S is used for floating potential (Floating), electron can be drawn out of charge accumulation layer 4a by the side of drain D.
If an electron is drawn out of only from charge accumulation layer 4b by the side of source S, a right voltage is impressed to source S and just to let drain D be floating potential.

[0142] Moreover, although illustration is not shown, read-out of a memory cell is performed by detecting the read-out current flowing between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) change according to the store status of the charge accumulation layers 4a and 4b. To which a bias shall be carried out should be selected from the source S or drain D where the modulation of current transfer characteristics appears notably.
According to four accumulation status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0143] Next, the method of manufacturing the memory cell of the non-volatile memory concerning the 10th embodiment of this invention is explained using the Fig. 93 to Fig. 101.
As first shown in Fig. 93 , the photo-resist pattern 27 is formed on the n-type-semiconductor substrate 19 except the field in which the channel field 25 is formed.
As shown in Fig. 94, etching the n-type-semiconductor substrate 19 by the RIE method forms a level difference 26.

[0144] Next, as shown in Fig. 95, the silicon nitride of small charge store capacity is deposited all over n-type-semiconductor substrate 19, and the 1st gate insulator layer 13 having about 10nm is formed.
Deposition of the silicon nitride film of small charge store capacity is performed for example, by the JVD method.
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the 2nd gate insulator layer 14 having about 5-10nm is formed.
Then, the silicon nitride of small charge store capacity is deposited by the JVD method, and the 3rd gate insulator layer 15 having about 10nm is formed.

[0145] Next, as shown in Fig. 96 , after depositing polycrystal silicon layer having the about 50-250nm in which n type or p type impurity is doped all over n-type-semiconductor substrate 19 by the LPCVD method, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then dry etching is carried out conformably to the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3 rd gate insulator layer 15 of the surface of the n-type-semiconductor substrate 19 of the field which uses the gate electrode 3 as a mask and forms a source field and a drain field.

[0146] Next, as shown in Fig. 97 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 alternatively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14. In the 10th embodiment of this invention, the 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide, and a fluoric acid system, for example, can be used as an etching reagent.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas containing HF gas instead of using the wet etching method which used the etching reagent.

[0147] Next, as shown in Fig. 98 , the silicon nitride 18 of high charge store capacity is accumulated all over n-type-semiconductor substrate 19 so that the space 17 for charge accumulation layer formation can be completely embedded by the LPCVD method.
And as shown in Fig. 99, anisotropic etching by RIE is performed to the whole surface of the n-type-semiconductor substrate 19, and the charge accumulation layers 4a and 4b which consisted of a silicon nitride of high charge store capacity are formed.

[0148] Next, as shown in Fig. 100, after forming an oxide film 16 all over n-type-semiconductor substrate 19, p- type diffusion layer 20 of low impurity concentration is formed. p- type diffusion layer 20 is formed by pouring p type impurity using the gate electrode 3 as the mask with ion-implantation technique and by activating the poured impurity with heat treatment.

[0149] Next, as shown in Fig. 101, after forming the sidewall spacer 9 in the sidewall of the gate electrode 3, p+ type diffusion layer 21 of high impurity concentration is formed.
The p+ type diffusion layer 21 is formed by pouring p type impurity using the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0150] Next, a high melting point metal film such as a tungsten, titanium and cobalt, is accumulated in the whole surface of the n type semiconductor circuit board 19, by the CVD or the spatter, then the electric conduction layer 12 composed of high melting point metal silicide is formed in each surface of the gate electrode 3 and the p+ type diffusion layer 21 by a n type semiconductor circuit board 19 being subjected to heat treatment in the inert atmosphere. If the high melting point metals of the un-response left in the territory except for the above is removed after the electric conduction layer 12 formation, the memory cell structure shown in the Fig. 90 can be completed.

[0151] In addition, although illustration is not shown, usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 90, and a final nonvolatile memory cell is completed.

[0152] Thus, in the 10th embodiment of this invention, the charge accumulation layers 4a and 4b can be formed in a self-matching target down the ends of the gate electrode 3.
Therefore, miniaturization of the orientation of gate length of a cell transistor is attained.
Thereby, large capacity and high-density nonvolatile semiconductor memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and nonvolatile semiconductor memory reduced sharply can be realized.

[0153] Moreover, the width of the charge accumulation layers 4a and 4b in the orientation of channel length can be easily controlled by adjustment of the etch-speed difference and etching time of the 1st gate insulator layer 13, the 3rd gate insulator layer 15 and the 2nd gate insulator layer 14.
Thereby, the charge accumulation layers 4a and 4b can be arranged symmetrically.
And since the charge accumulation layers 4a and 4b are electrically separated completely by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b do not happen.
Furthermore, since the charge accumulation layers 4a and 4b are insulated completely from a source field, a drain field, the gate electrode 3, and a channel field by the 1st insulator layer 13 and the 3rd insulator layer 15, and the oxide film 16, the nonvolatile semiconductor memory which was excellent in the charge hold property can be provided.
The charge accumulation layers 4a and 4b are formed in the orientation of a channel field from the edge of the gate electrode 3 and the current transfer-characteristics of the memory cell is almost decided by the charge store status of the side portion of the channel field of the charge accumulation layers 4a and 4b.
Therefore, if the length of the orientation of gate length of this portion is reduced to a limitation,

more detailed nonvolatile semiconductor memory can be provided.

[0154] Furthermore, since the cell structure is easily realizable at usual CMOS process, the nonvolatile semiconductor memory can be manufactured by the low cost using the existing production line.

[0155] And with the 10th embodiment of this invention, the electron-injection luminous efficacy at the time of writing can be raised.
For this reason, improvement in the speed and reduction of the applied voltage at the time of writing can be attained.

[0156](11th Embodiment Form) Next, the 11th embodiment form of this invention is explained.
In the 10th embodiment form of the above, the 11th embodiment of this invention makes unnecessary the 2nd insulator layer 14 arranged between charge accumulation layer 4a of Fig. 90, and charge accumulation layer 4b, and has taken the configuration which made two charge accumulation layers 4a and 4b unify.
Fig. 102 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 11th embodiment of this invention.
As shown in Fig. 102 , this memory cell structure is changed to the charge accumulation layers 4a and 4b of the 10th embodiment form of the above, and the 2nd insulator layer 14, and arranges charge accumulation layers 4f.

[0157] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 11th embodiment of this invention is explained using the Fig. 103 to the Fig. 108 .
Like the 10th embodiment of the above, as first shown in Fig. 103 , the photo resist pattern 27 is formed except the field in which the channel field 25 is formed on the n-type-semiconductor substrate 19.
And as shown in Fig. 104, a level difference 26 is formed by etching the n-type-semiconductor substrate 19 by the RIE method.

[0158] Next, as shown in Fig. 105 , the small silicon nitride of charge store capacity is deposited all over n-type-semiconductor substrate 19, and the about 10nm 1st gate insulator layer 13 is formed.
Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD method.
About 5-10nm of the high silicon nitrides 18 of charge store capacity is formed by the LPCVD method after 1st gate insulator layer 13 formation. Then, the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0159] Next, as shown in Fig. 106 , after depositing the polycrystal silicon layer having about 50 - 250nm in which n type or p type impurity is doped by the LPCVD method all over n-type-semiconductor substrate 19, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then dry etching is carried out conformably to the 1st gate insulator layer 13, the silicon nitride 18, and the 3rd gate insulator layer 15, of the surface of the n-type-semiconductor substrate 19 of the field which uses the gate electrode 3 as a mask and forms a source field and a drain field.
Here, charge accumulation layer 4f is formed.

[0160] Next, as shown in Fig. 107, after forming an oxide film 16 all over n-type-semiconductor substrate 19, p- type diffusion layer 20 of low impurity concentration is formed.
The p- type diffusion layer 20 is formed by pouring p type impurity using the gate electrode 3 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0161] Next, as shown in Fig. 108, after forming the sidewall spacer 9 in the side attachment wall

of the gate electrode 3, of high impurity concentration is formed.
The p+ type diffusion layer 21 is formed by pouring p type impurity using the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0162] Next, high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the n-type-semiconductor substrate 19, then the n-type-semiconductor substrate 19 is heat-treated in an inert atmosphere, thereby forming the electric conduction layer 12 which consists of a refractory-metal siliside on each surface of the gate electrode 3 and p+ type diffusion layer 21.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 102 will be completed.

[0163] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 102 , and a final nonvolatile memory cell is completed.

[0164] (12th Embodiment Form) Next, the 12th embodiment form of this invention is explained. Fig. 109 is a cross section showing the structure of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.
Although exposure technique and etching technique were used for patterning of the gate electrode 3 with the 10th embodiment of the above, it is the example which uses the chemical mechanical grinding method for patterning of the gate electrode 3 in the 12th embodiment.

[0165] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 12th embodiment form of this invention is explained using the Fig. 110 to the Fig. 118 . As first shown in Fig. 110 , the photoresist pattern 27 is formed except the field in which the channel field 25 is formed on the n-type-semiconductor substrate 19.
And as shown in Fig. 111 , a level difference 26 is formed by etching the n-type-semiconductor substrate 19 by the RIE method.

[0166] Next, as shown in Fig. 112 , the small silicon nitride of charge store capacity is deposited all over n-type-semiconductor substrate 19, and the about 10nm 1st gate insulator layer 13 is formed.
Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD method.
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.
Furthermore, the about 50-500nm polycrystal silicon layer 28 which doped n type or p type impurity by the LPCVD method all over n-type-semiconductor substrate 19 is deposited.

[0167] Next, as shown in Fig. 113 , the gate electrode 3 is formed by embedding the polycrystal silicon layer 19 by the chemical mechanical polishing technique. In addition, wet etching usually removes the 1st gate insulator layer 13, the 2nd gate insulator layer 14, and the 3rd gate insulator layer 15 which remain on the n-type semiconductor substrate 19.

[0168] Next, as shown in Fig. 114 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 alternatively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14.

What is necessary is just to use for example, a fluoric acid system as an etching reagent with the 12th embodiment form of this invention, since it reaches 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas.

[0169] Next, as shown in Fig. 115 , it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over n-type-semiconductor substrate 19.
And as shown in Fig. 116 , anisotropic etching by RIE is performed to the n-type-semiconductor substrate 19 whole surface, and the charge accumulation layers 4a and 4b which consisted of a high silicon nitride of charge store capacity are formed.

[0170] Next, as shown in Fig. 117 , after forming an oxide film 16 all over n- type semiconductor substrate 19, p- type diffusion layer 20 of low impurity concentration is formed. It forms by activating the impurity which p- type diffusion layer 20 used the gate electrode 3 as the mask with ion-implantation technique, poured in p type impurity, and was poured in with subsequent heat treatment.

[0171] Next, as shown in Fig. 118 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, p+ type diffusion layer 21 of high impurity concentration is formed.
The p+ type diffusion layer 21 is formed by pouring p type impurity using used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0172] Next, the thing for which high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the n-type-semiconductor substrate 19, then the n-type-semiconductor substrate 19 is heat-treated in an inert atmosphere. Thereafter the electric conduction layer 12 which consists of a refractory-metal silicide is formed on each surface of the gate electrode 3 and p+ type diffusion layer 21.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 109 will be completed.

[0173] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 109 , and a final nonvolatile memory cell is completed.

[0174] (13th Embodiment Form) Next, the 13th embodiment form of this invention is explained.
With the embodiment of the above-mentioned 1st to the 12th above-mentioned embodiment, sufficient study to improvement in the speed of transistors other than a memory cell was not made.
On the other hand, as structure of a high-speed CMOS transistor, by forming the notch on concave between a gate electrode and a source drain diffusion layer, the capacity between a gate electrode and a diffusion layer is reduced, and the attempt, which accelerates the logic gate, is made (T.Ghani et al., IEDM99, and p415).
In this 13th embodiment form, this structure is used for nonvolatile semiconductor memory, and enables large improvement in the speed of the semiconductor device that contains the usual transistor which does not have a memory and usual nonvolatile semiconductor memory.

[0175] Fig. 119 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention.

This memory cell consists of an n type MOS transistor. With the memory cell structure of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention, the gate electrode 3 is formed in the surface of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
A concavity is prepared in the ends of the gate electrode 3, and the charge accumulation layer 4 (4a, 4b) is formed in each concavity.
The oxide film 30 is formed between the charge accumulation layer 4 and the gate electrode 3.
The sidewall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and n+ type diffusion layer 11.

[0176] The memory cell of the non-volatile memory concerning the 13th embodiment form of this invention has LDD structure which constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration. And the charge accumulation layer 4 (4a, 4b) is formed in the both ends of the gate electrode 3. An electron is accumulated to these two charge accumulation layers 4a and 4b. The store status are four possibility

(1) Neither charge accumulation layer 4a nor 4b is accumulating the electron,
(2) only charge accumulation layer 4a is accumulating the electron, the status that only
(3) only charge accumulation layer 4b is accumulating the electron
(4) Both charge accumulation layers 4a and 4b are accumulating the electron.

The amount of the change of threshold potential produced by the existence of the electron held at these two charge accumulation layers 4a and 4b is made to correspond to a storage information "00", "01", "10", and "11."
Moreover, with this memory cell structure, since the charge accumulation layer 4 is located in the upper part of a channel field edge, the threshold voltage of a channel field center section is decided only by impurity concentration of a channel field, and it does not depend for it on the store status of the electron of the charge accumulation layer 4.
Therefore, the fault deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layer 4 is prevented, and the poor leakage which originates in a fault deletion by that cause, a poor program, and poor read-out must have been produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and can realize highly reliable non-volatile memory.
What is necessary is for the charge accumulation layer 4 just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membranous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
If the 1st gate insulator layer 13 is furthermore constituted from a silicon nitride (Si_3N_4 layer) which has the dielectric constant of an about 2 times of a silicon oxide (SiO_2 layer), a silicon-oxide conversion thickness can stabilized and the very thin gate insulator layer which is from about 4nm to 11nm can be realized.
For example, since the real thickness in 5nm of the silicon nitride whose silicon-oxide conversion thickness is about 10nm, the induction of the direct tunnel (DT) injection is not carried out.
Therefore, the voltage at the time of an electronic injection extraction operation is reduced in low-battery, and not only miniaturization of a memory cell but miniaturization of a circumference high-voltage operation element of it is attained.

[0177] Although n- type diffusion layer 10 is established for the purpose of the pressure-proof enhancement in a source field and a drain field and LDD structure is constituted from a memory

cell of the non-volatile memory concerning the 13th embodiment form of this invention, a source field and a drain field may consist of single drain structure and double drain structure.

[0178] Next, an operation of the non-volatile memory concerning the 13th embodiment form of this invention is explained using the Fig. 120 and the Fig. 121 . Fig. 120 is a cross section of the non-volatile memory explaining a write-in operation. Fig. 121 is a cross section of the non-volatile memory explaining a deletion operation.
The memory cell of the Fig. 120 and the Fig. 121 consists of an n type MOS transistor.
As shown in Fig. 120 , at the time of the writing of a memory cell, voltage of about 6-8V is impressed to gate G, voltage of about 4-5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field by the channel thermo electron (CHE). What is necessary is just to replace with the above the voltage impressed to drain D and each source S, in pouring an electron into charge accumulation layer 4b by the side of a source field.
On the other hand, as shown in Fig. 121 , a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by Fig. out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when two or more memory cells share gate G, an electron can be simultaneously drawn out from those memory cells. In this case, source S and drain D should just be taken as the p type semiconductor substrate 1 and this potential.
Moreover, it is also possible to impress the right voltage different from the potential of the p type semiconductor substrate 1 to a drain electrode, and to draw out an electron for a source electrode only from floating potential (Floating), then charge accumulation layer 4b by the side of a drain electrode.
What is necessary is to impress a right voltage to a source electrode, in drawing out an electron only from charge accumulation layer 4a by the side of a source electrode, and just to let a drain electrode be floating potential.

[0179] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current flowing between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0180] Next, the operation of the non-volatile memory concerning the 13th embodiment form of this invention which consists of a p type MOS transistor is explained using the Fig. 122 and the Fig. 123.
Fig. 122 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 123 is a cross section of the non-volatile memory explaining a deletion operation.
The memory cell of the Fig. 122 and the Fig. 123 consists of a p type MOS transistor.
As shown in Fig. 122, at the time of the writing of a memory cell, about 5V is impressed to gate G, and about -5V is impressed to drain D, respectively, and let source S be floating potential.
Thus, a voltage is impressed, energy is given the electron of the tunnel phenomenon reason between band-bands by the electric field near the drain field, and an electron is poured into charge accumulation layer 4b by the side of a drain field.
What is necessary is just to replace with the above the voltage impressed to drain D and each source S, in pouring an electron into charge accumulation layer 4a by the side of a source field.
On the other hand, as shown in Fig. 123 , a deletion of a memory cell is carried out by impressing a negative voltage (at least -5V) to gate G and drawing an electron from the charge accumulation layers 4a and 4b using FN current.

Moreover, when two or more memory cells share gate G, an electron can be simultaneously drawn out from those memory cells. In this case, source S and drain D are taken as the n-type-semiconductor substrate 19, this potential, or floating potential.

[0181] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current flowing between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0182] In the 13th embodiment form of this invention, the usual MOS transistor as shown in Fig. 124, which does not have a memory, is also realizable.
Because, in this MOS transistor, the charge accumulation layer 4 is arranged only on the source drain field 10 and 11, and is not arranged on the channel field.
For this reason, the conduction property of this MOS transistor is because influence is not received in the hold status of the charge of the charge accumulation layer 4 at all.
Furthermore, by presence of the concavity of the gate electrode 3, the parasitic capacitance between gate-source drains is reduced and it also has the advantageous point that the fast turn around of an MOS transistor becomes possible.

[0183] (14th Embodiment Form) Next, the 14th embodiment form of this invention is explained.
The 14th embodiment form serves as the configuration of having made the charge accumulation layer 4 and the sidewall spacer 9 unifying, in the 13th embodiment form of the above.
Fig. 125 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention.
This memory cell consists of an n type MOS transistor.
With the memory cell structure of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention, the gate electrode 3 is formed in the surface of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
A concavity is prepared in the ends of the gate electrode 3, and the charge accumulation layer 4 (4a, 4b) is formed in each concavity.
The oxide film 30 is formed between the charge accumulation layer 4 and the gate electrode 3.
The sidewall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and a part of this sidewall spacer 9 constitutes the charge accumulation layer 4. n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of the sidewall spacer 9.
The electric conduction layer 12 is formed in each surface of gate electrode 3 and n+ type diffusion layer 11.

[0184] What is necessary is for the 14th embodiment form of this invention just to constitute the sidewall spacer 9 and the charge accumulation layer 4 from the high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the film quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.

[0185] In the 14th embodiment form of this invention, a usual MOS transistor as shown in Fig.

126 is realizable as well as the 13th embodiment of the above

[0186]
[Effect of the Invention] According to this invention, the structure of the nonvolatile semiconductor memory, which can memorize the information for two or more bits by the easy cellular structure, is realizable.

[0187] According to this invention, the manufacture technique of the nonvolatile semiconductor memory which manufactures the nonvolatile semiconductor memory, which memorizes the information for two or more bits in an easy manufacture process, is realizable.

[0188] According to this invention, the structure of a semiconductor memory containing non-volatile memory capable of electrically writing/deleting and volatile memory capable of high-speed writing in and reading out, is realizable with a simple cell structure.

[0189] According to this invention, the manufacture technique of a semiconductor memory containing non-volatile memory capable of electrically writing/deleting and volatile memory capable of high-speed writing in/reading out, is realizable with simple manufacture process.

[Brief Description of the Drawings]
[Fig. 1] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 2] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 3] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 4] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 5] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 6] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 7] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 8] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 9] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 10] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 11] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 12] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 13] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 14] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 15] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 16] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 17] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 18] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 19] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 20] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.

[Fig. 21] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.

[Fig. 22] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.

[Fig. 23] It is the cross section showing the structure of the MOS transistor which constitutes the circumference circuit of the non-volatile memory concerning the 5th embodiment form of this invention.

[Fig. 24] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 25] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 26] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 27] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 28] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 29] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 30] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 31] It is the cross section showing the memory cell structure of the nonvolatile

semiconductor memory carried in the semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 32] It is the cross section showing the memory cell structure of the volatile semiconductor memory carried in the semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 33] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 34] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 35] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 36] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 37] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 38] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 39] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 40] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 41] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 42] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 43] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 44] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 45] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 46] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 47] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 48] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 49] It is the cross section showing the manufacturing process of the memory cell of the

volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 50] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 51] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 52] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 53] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory carried in the semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 54] It is the cross section showing the memory cell structure of the volatile semiconductor memory carried in the semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 55] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 56] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 57] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 58] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 59] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 60] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 61] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 62] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 63] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 64] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 65] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 66] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 67] It is the cross section showing the manufacturing process of the memory cell of the

volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 68] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 69] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 70] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 71] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 72] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 73] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 74] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 75] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 76] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 77] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 78] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 79] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 80] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 81] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 82] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 83] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 84] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 85] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 86] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 87] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 88] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 89] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 90] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 91] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 92] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 93] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 94] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 95] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 96] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 97] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 98] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 99] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 100] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 101] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 102] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 103] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 104] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 105] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 106] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 107] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 108] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 109] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 110] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 111] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 112] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 113] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 114] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 115] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 116] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 117] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 118] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 119] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention.

[Fig. 120] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of an n type MOS transistor.

[Fig. 121] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of an n type MOS transistor.

[Fig. 122] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of a p type MOS

transistor.

[Fig. 123] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of a p type MOS transistor.

[Fig. 124] It is the cross section showing the structure of the MOS transistor which has the same gate structure as the memory cell of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention.

[Fig. 125] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention.

[Fig. 126] It is the cross section showing the structure of the MOS transistor which has the same gate structure as the memory cell of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention.

[Description of Notations]
1 P Type Semiconductor Substrate
2 Gate Insulator Layer
3 Gate Electrode (1st Gate Electrode)
4 Charge Accumulation Layer
5 1st Oxide Film
6 Nitride
7 2nd Oxide Film
8 2nd Gate Electrode
9 Sidewall Spacer
10 N- Type Diffusion Layer
11 N+ Type Diffusion Layer
12 Electric Conduction Layer
13 1st Gate Insulator Layer
14 2nd Gate Insulator Layer
15 3rd Gate Insulator Layer
16 Oxide Film
17 Space for Charge Accumulation Layer Formation
18 Silicon Nitride
19 N-type-Semiconductor Substrate
20 P- Type Diffusion Layer
21 P+ Type Diffusion Layer
22, 27 Photoresist (photoresist pattern)
23 Tunnel Insulator Layer
24 4th Gate Insulator Layer
25 Channel Field
26 Level Difference
28 Polycrystal Silicon Layer